

VDKTE

Rosetta 10ADT/10ADTG

LA-9869P REV 0.3 Schematic

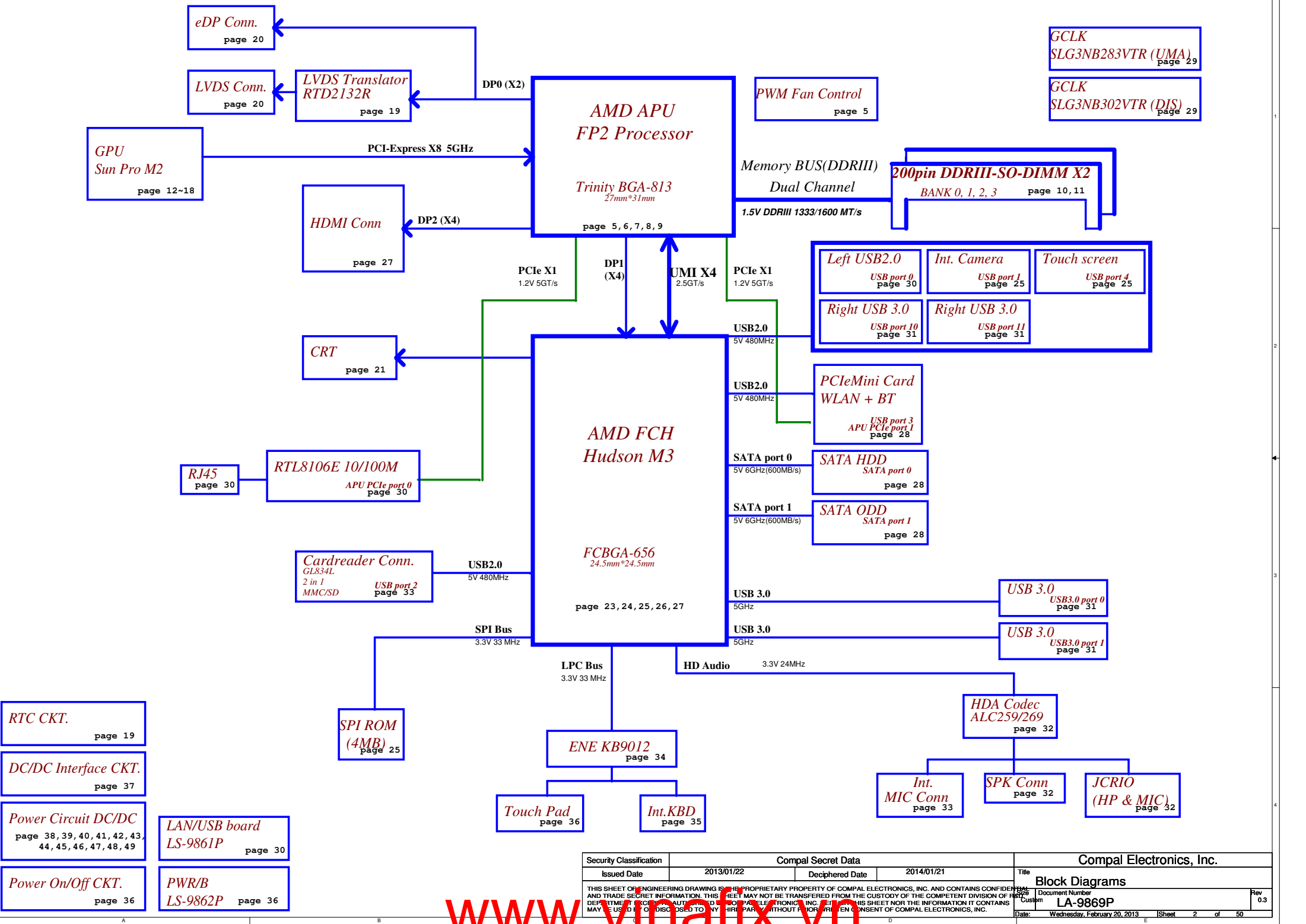
AMD APU RICHLAND FP2 / FCH BOLTON-M3

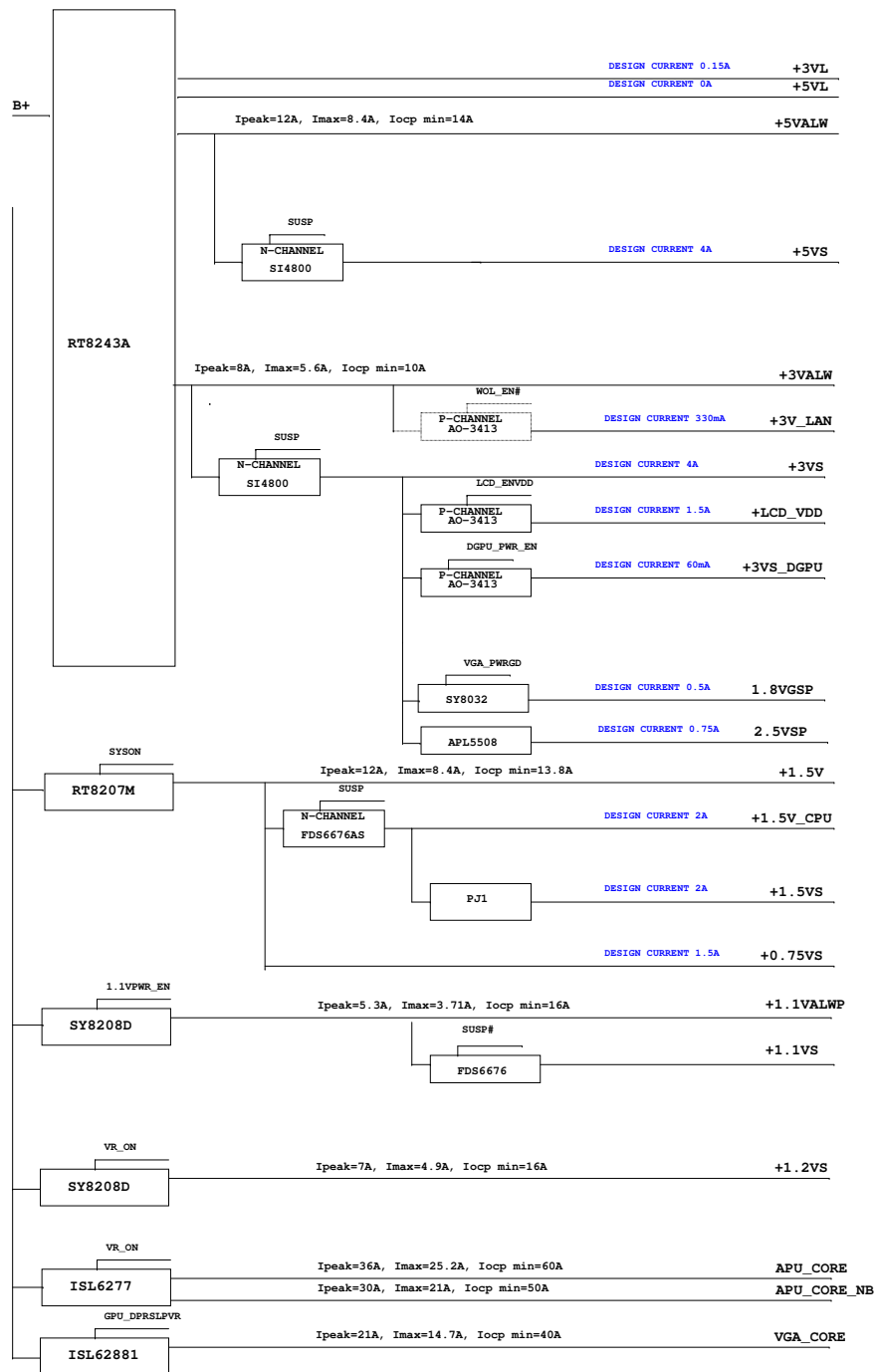
Sun Pro M2

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2013-02-20 Rev 0.3

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +1.1VALW
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	APU		FCH		GPU	
description			Bolton			
explain	R1	R3	R1	R3	R1	R3
BTO			BOLTONR1@	HUDM3R3@		

Function	3D sensor	KB LED	Clock		UMA/DIS	
description		K			1G	U
explain	G-sensor	KB LED	Green Clock	No Green Clock	DIS	UMA
BTO	GSENSOR@	KBL@	GCLK@	NOGCLK@	VGA@	UMA@

Function	Panel			
description	S	D		
explain	LVDS	eDP		
BTO	LVDS@	IEDP@		

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 000X b
+3VS	DDR SO-DIMM 1	A2 H	1010 001X b
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Charger	12 H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VL	SB-TSI	98 H	1001 1001 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	VGA Thermal	82H	1000 0010 b

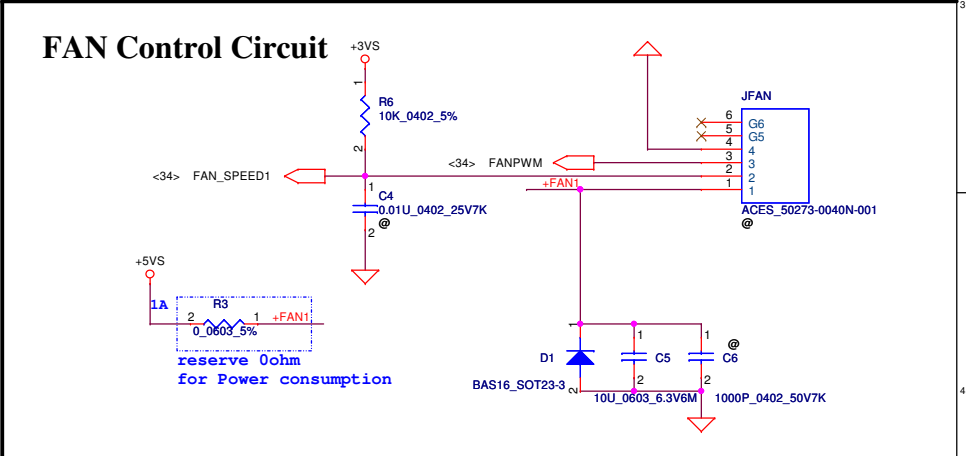
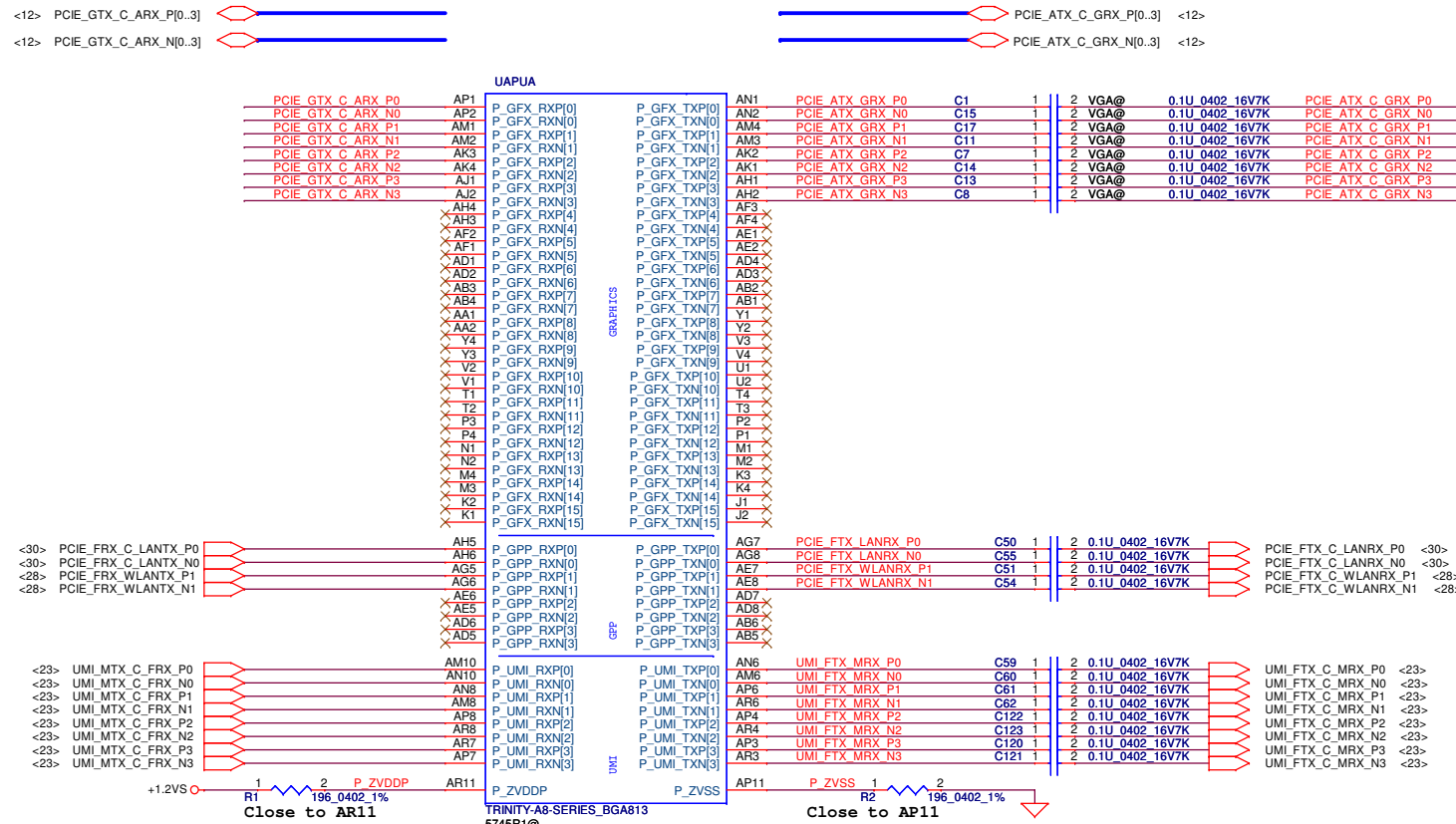
EC SM Bus3 Address

Power	Device	HEX	Address
+3VS	LVDS Translator	94 H	1001 0100 b

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

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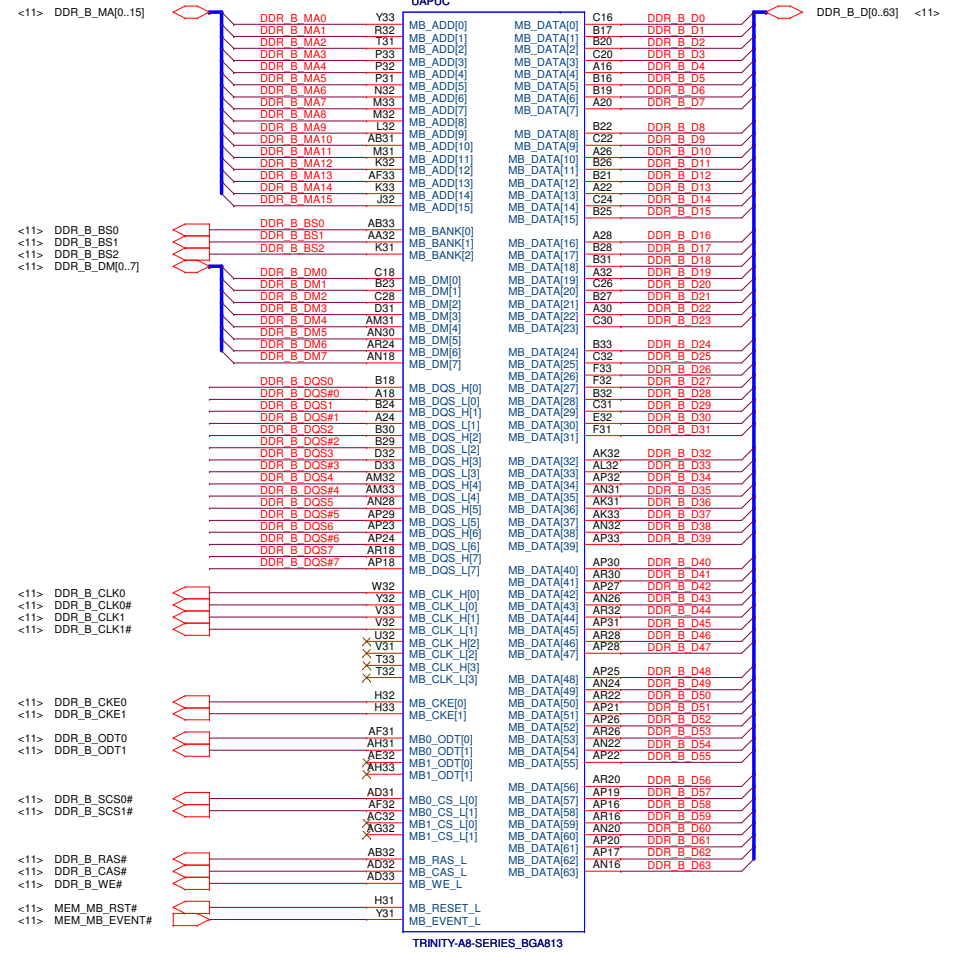
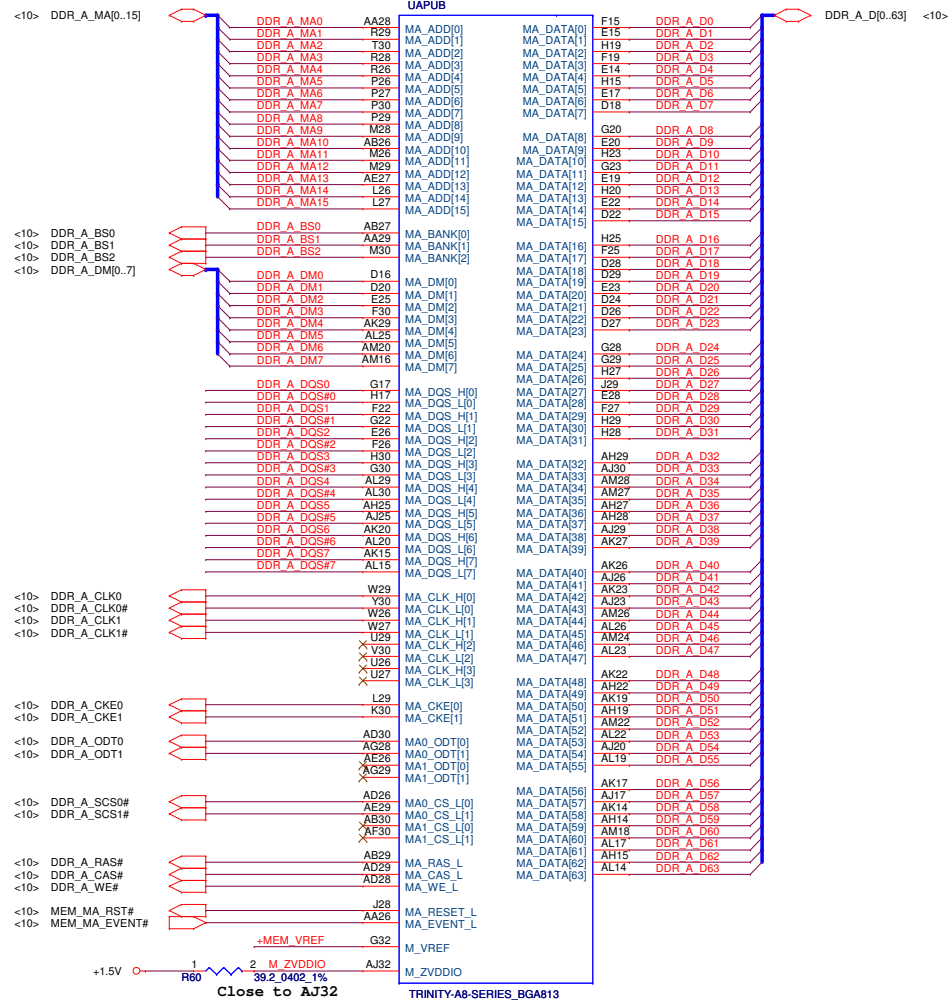
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<10> DDR_A_DQS[0..7]

<10> DDR_A_DQS# [0..7]

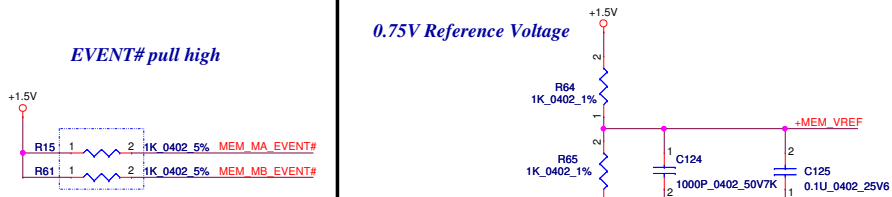
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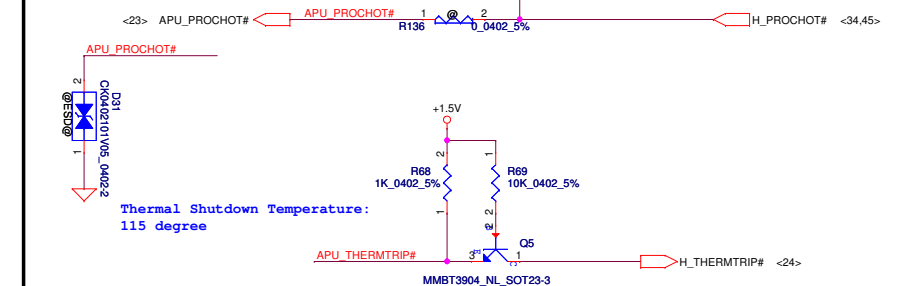
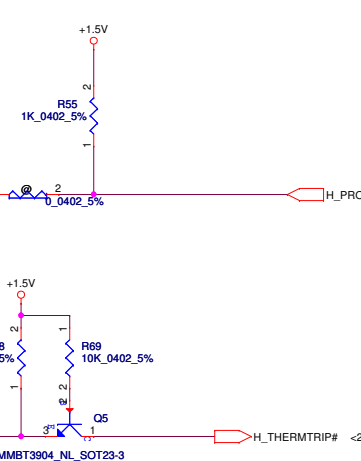


EVENT# pull high

0.75V Reference Voltage

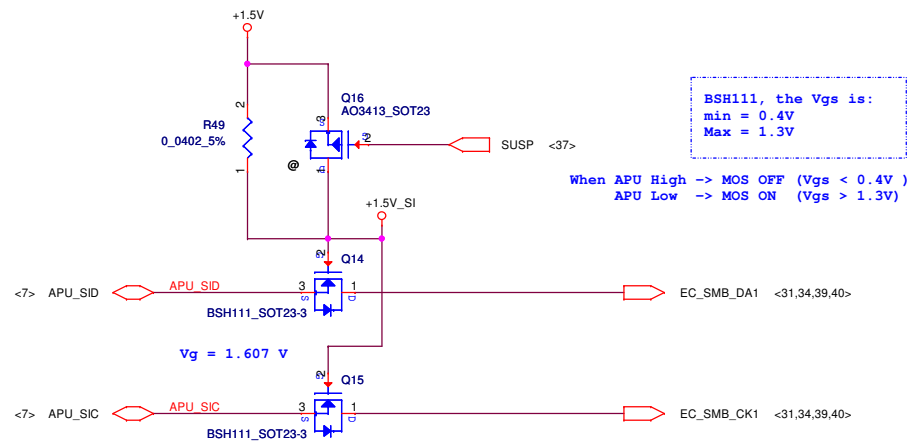


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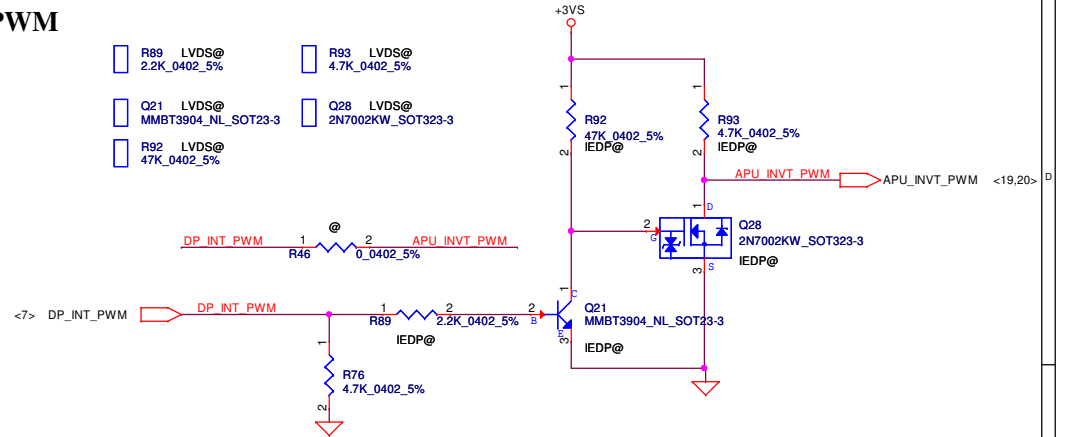


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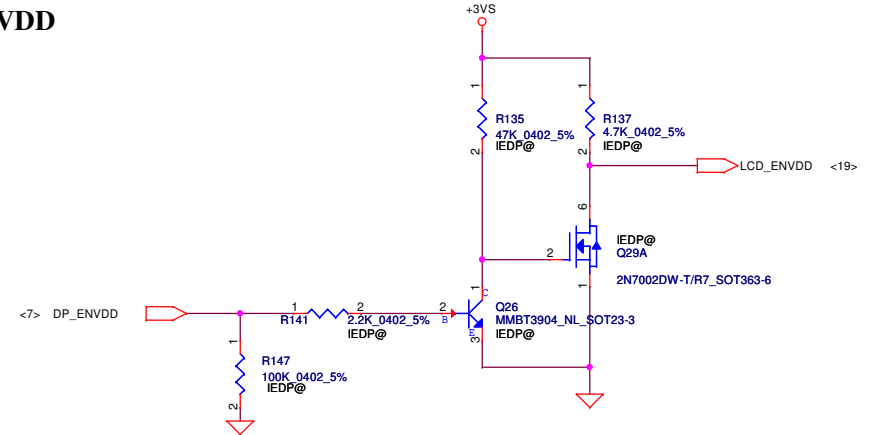
SB-TSI



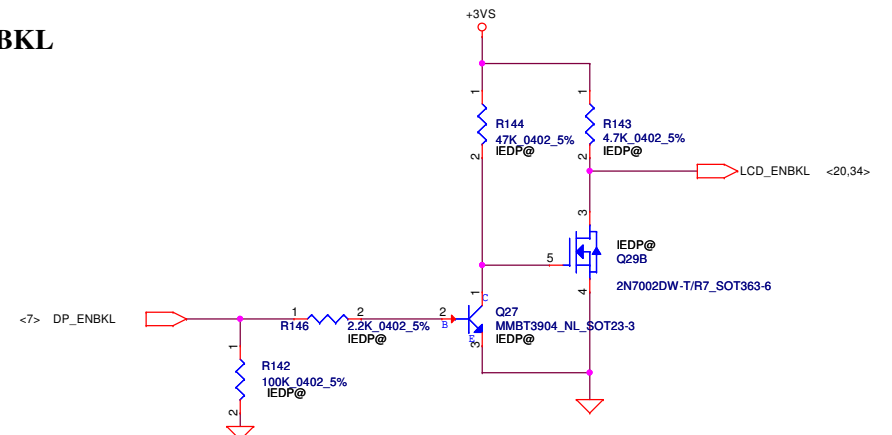
Panel PWM



eDP Panel ENVDD

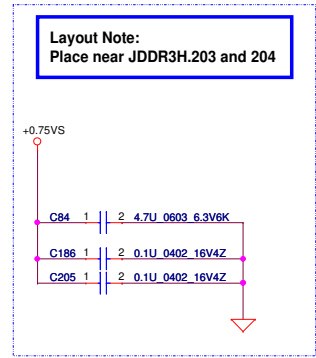
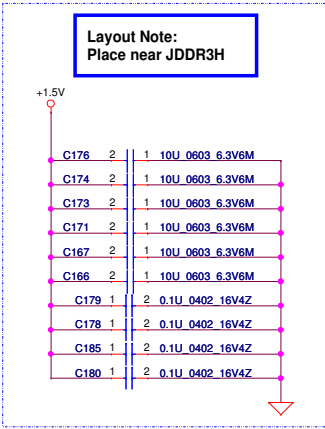
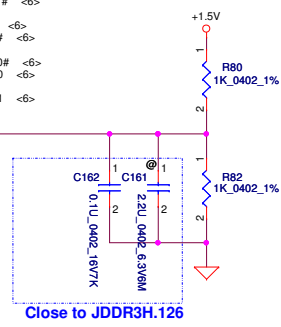
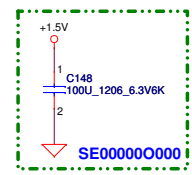
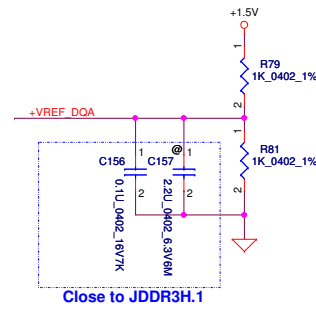
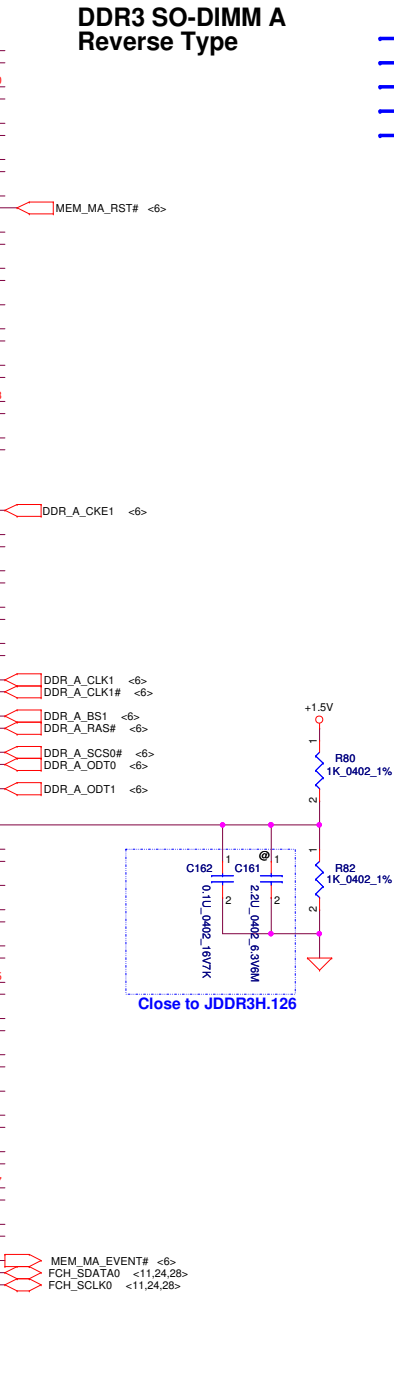
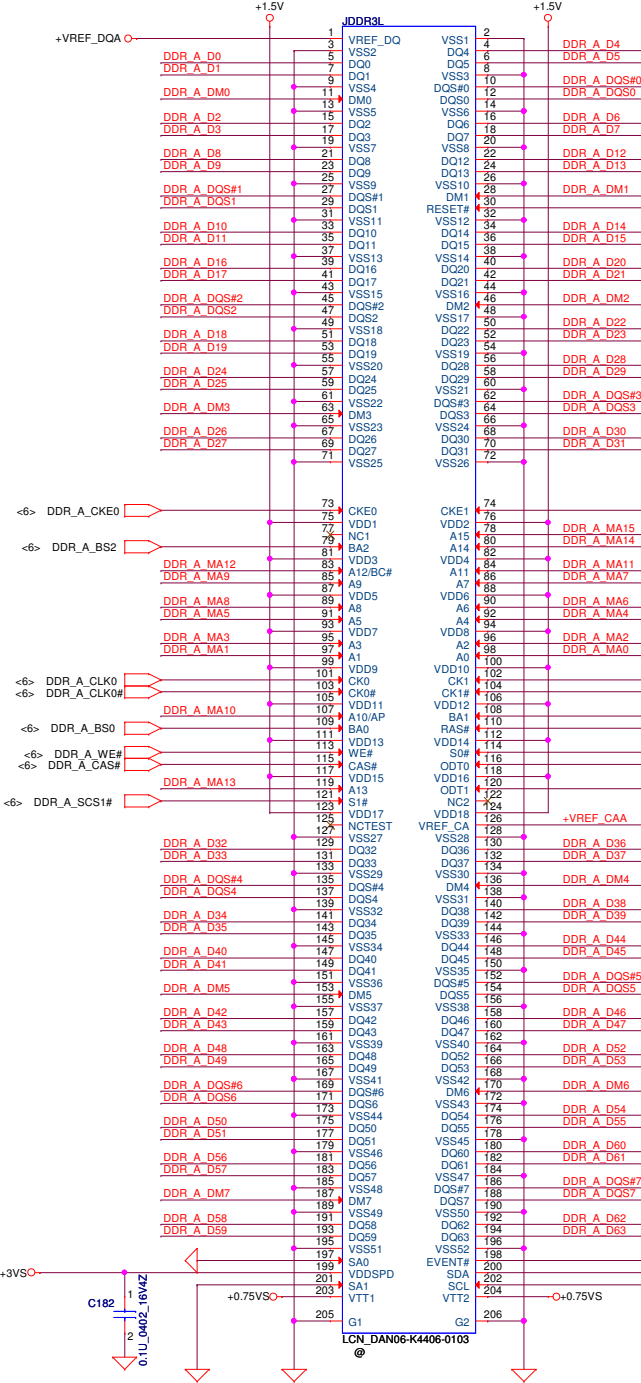
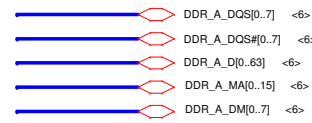


eDP Panel ENBKL



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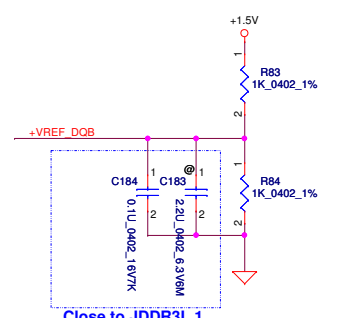
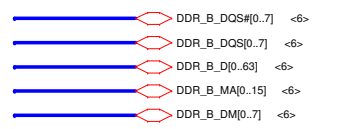
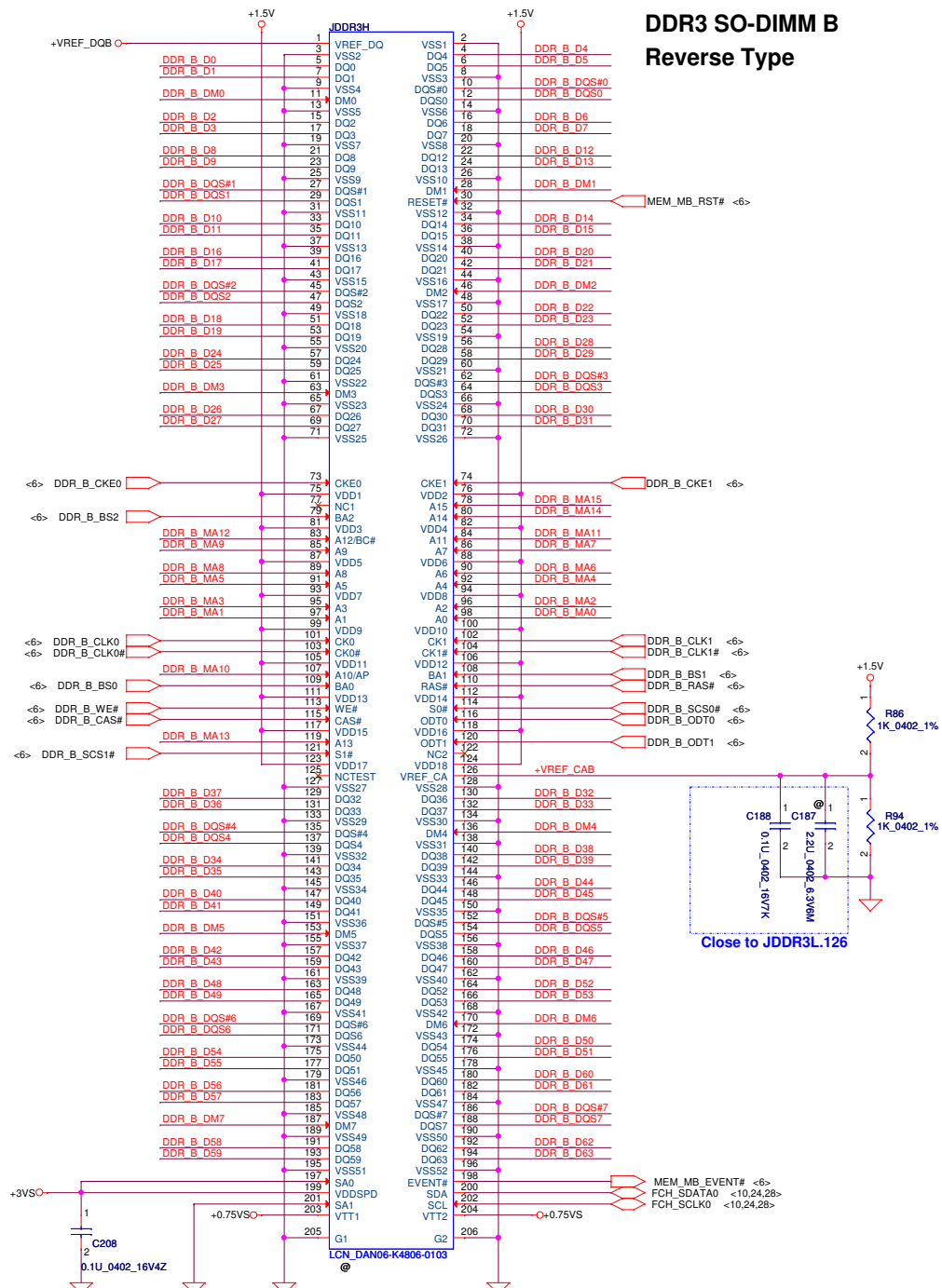
DDR3 SO-DIMM A Reverse Type



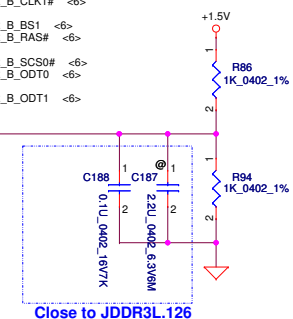
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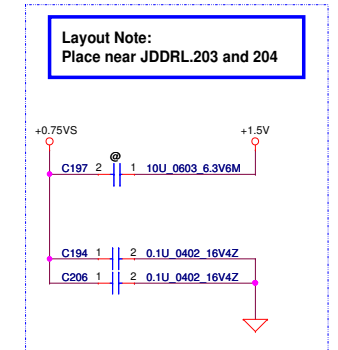
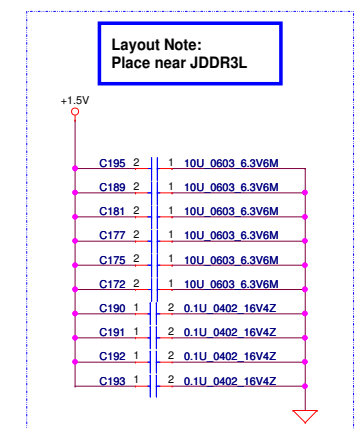
DDR3 SO-DIMM B Reverse Type

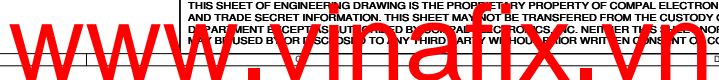


Close to JDDR3L.1



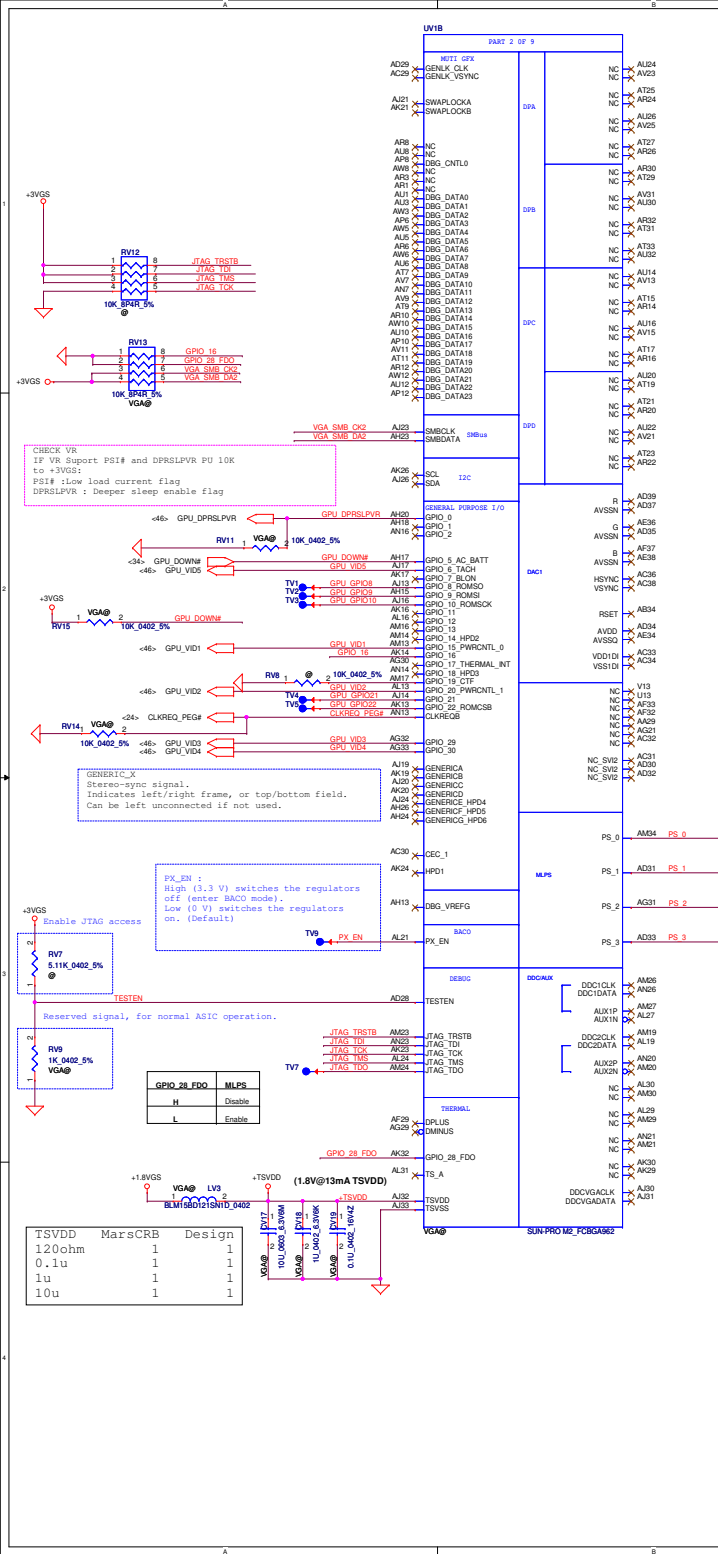
Close to JDDR3L.126





PART 7 OF 9		
LVDS CONTROL		
LVDS0P	TXCBP_DPB3P	AK35 AL36
	TXCBM_DPB3N	AK27 AJ27
	TX3P_DPB2P	AJ38 AK37
	TX3M_DPB2N	AJ36
	TX4P_DPB1P	AH35 AJ36
	TX4M_DPB1N	AG38 AH37
	TX5P_DPB0P	AF35 AG36
	NC#AF35	
	NC#AG38	
	TXCAP_DPA3P	AP34 AR34
	TXCAM_DPA3N	
	X0P_DPA2P	AW37 AU35
	X0M_DPA2N	
	TX1P_DPA1P	AR37 AU39
	TX1M_DPA1N	
	TX2P_DPA0P	AP35 AR35
	TX2M_DPA0N	
	NC	AN36 AP37
	NC	

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Mars MLPS configuration			
Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.99k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

Primary Memory Aperture Size Requested at PCI Configuration			
Size of the Primary Memory Apertures	ROM_CONFIG [2:0]		
128 MB	000		
256 MB	001		
64 MB	010		
Reserved	011		
512 MB	Not supported		
1 GB	Not supported		
2 GB	Not supported		
4 GB	Not supported		

Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3 V (VDD33)	PD-reset	Power-state indicator. Permits the voltage regulator to activate power-saving features. If VR Support PS1# and DPRSLPVR PU 10K to +3VGS. PS1# : low load current flag DPRSLPVR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O 3.3 V (VDD33)	PD-reset	(Optional) An input which allows the system to request a fastpower reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods in order to prevent display disturbances.
GPIO_6	I/O 3.3 V (VDD33)	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be inputs with weak internal pull-down resistors. The VBIOS can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD Powerplay state when they are used as voltage control signals. Note: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_10_ROMSD	I 3.3 V (VDD33)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output.
GPIO_9_ROMSI	I 3.3 V (VDD33)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK	O 3.3 V (VDD33)	PD-reset	Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB	O 3.3 V (VDD33)	PD-reset	BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. Design: No use external VGA ROM, so use the test points
GPIO_17_THERMAL_INT	I/O 3.3 V (VDD33)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb).
GPIO_19_CTF	O 3.3 V (VDD33)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTF setpoint is 109°C by default, and is programmed during ASIC initialization. See the advisory for AMD Powerplay states for more details.
GPIO_21	I/O 3.3 V (VDD33)	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_28_FDO	I/O 3.3 V (VDD33)	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
CLKREQB	O		Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock to the ASIC. On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERST# is deasserted.
PX_EN	O	PD	

MLPS

MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1]	ROM_CONFIG[0]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYN	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO_8	Re-defined strap to indicate PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	BIF_VGA_DIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1]	BOARD_CONFIG[0]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_3[2]	BOARD_CONFIG[1]	N/A		
PS_3[3]	BOARD_CONFIG[2]	N/A		
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable.	111
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	N/A		
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	N/A		

For MEMCLK 1GHz	brand	Description	Comment	PS_3[3:1]	R _{pu} (ohm)	R _{pd} (ohm)
gDDR3-2Gbit	skhynix	H5TQ2G63DFR-N0C	1.5V/1GHz	000	NC	4750
	Samsung	K4W2G1646E-BC1A	1.5V/1GHz	111	4750	NC

For MEMCLK 900MHz	brand	Description	Comment	PS_3[3:1]	R _{pu} (ohm)	R _{pd} (ohm)
gDDR3-2Gbit	skhynix	H5TQ2G63DFR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-1070:K	1.35V-1.5V/900MHz	001	8450	2000
	Samsung	K4W2G1646E-MC11	1.5V/900MHz	111	4750	NC

MLPS Strap

Bits[5:1]	Bits[3:1]	Capacitor	R _{pu}	R _{pd}
PS_0[5:1]	1 1 0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1 0 0 1	NC	8.45K	2K
PS_2[5:1]	0 0 0 0 0	880 nF	NC	475K
PS_3[5:1]	1 1 XXX	NC	X	X

Mapping to VRAM type please refer to page 6

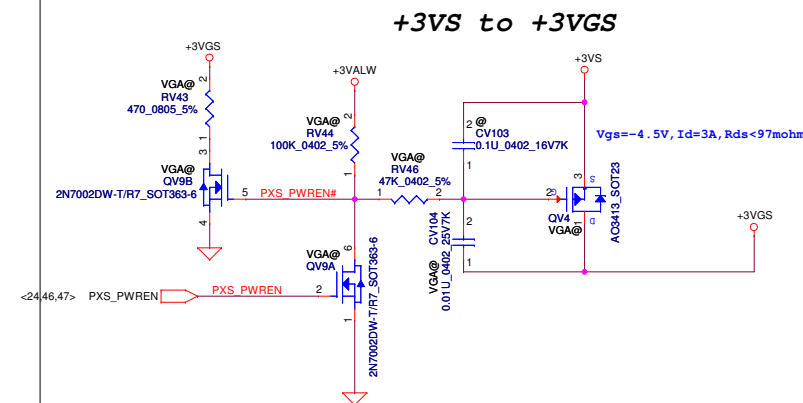
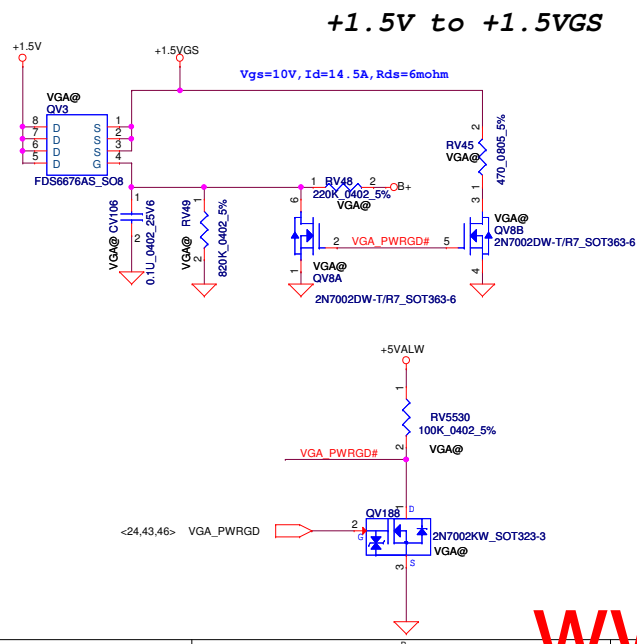
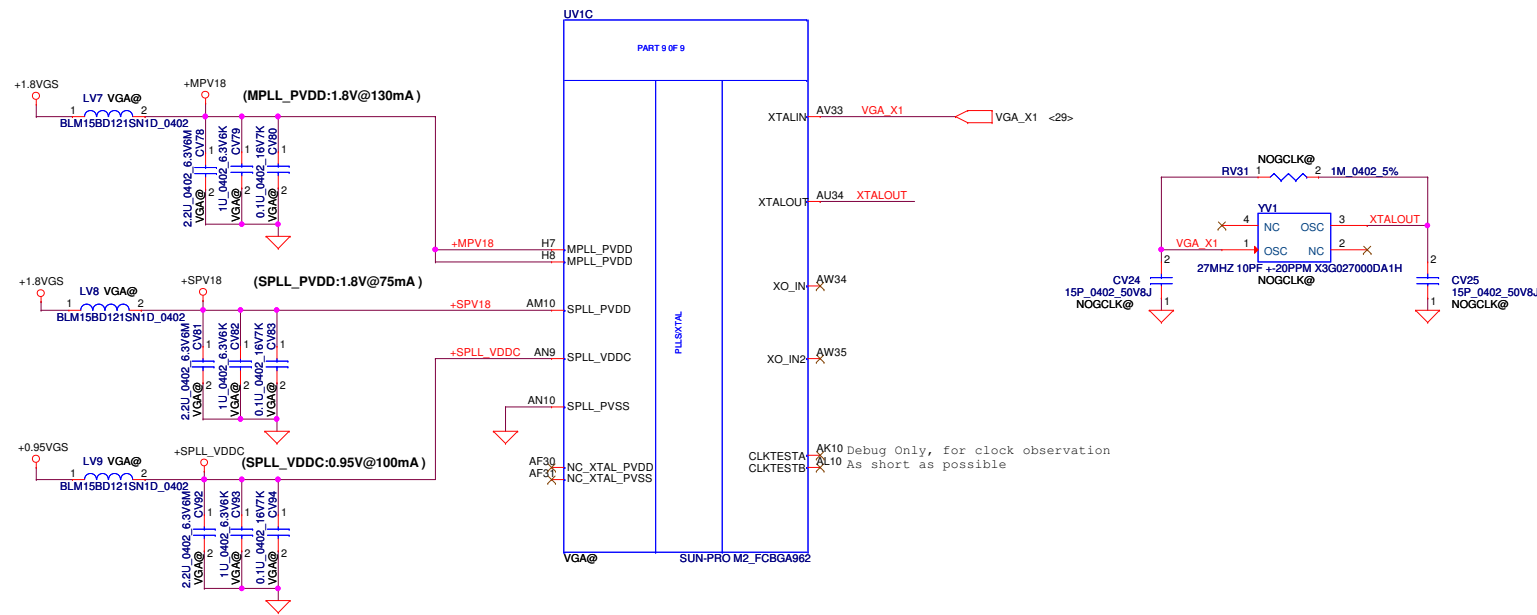
Compul Secret Data			
Security Classification	2013/01/22	Deciphered Date	2014/01/21
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compul Electronics, Inc.			
Main MSIC			
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Size	Document Number	Rev	0.3
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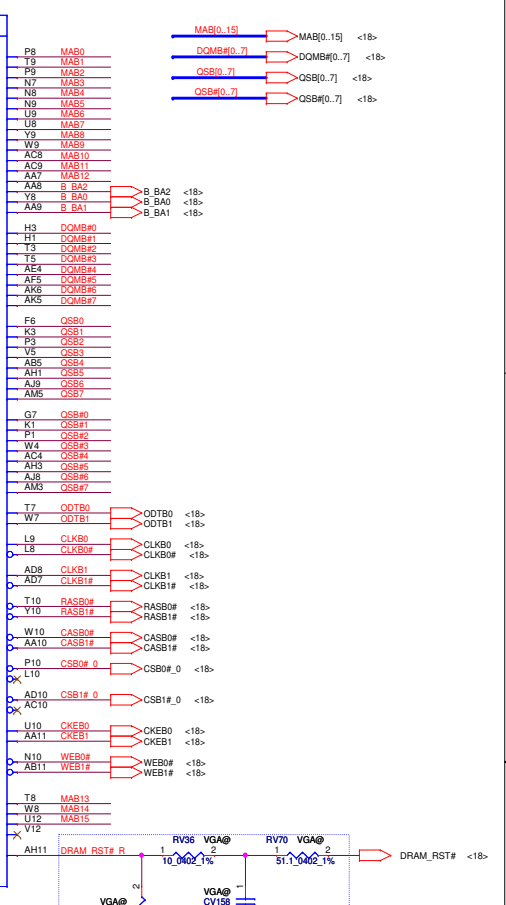
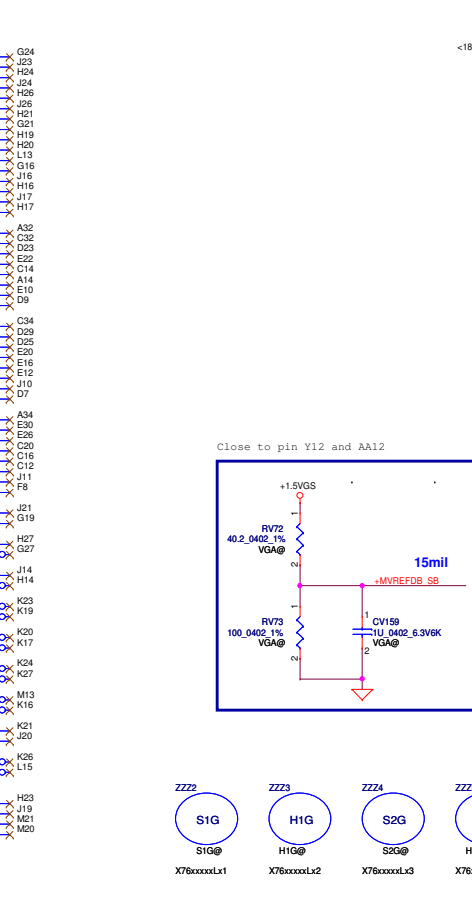
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

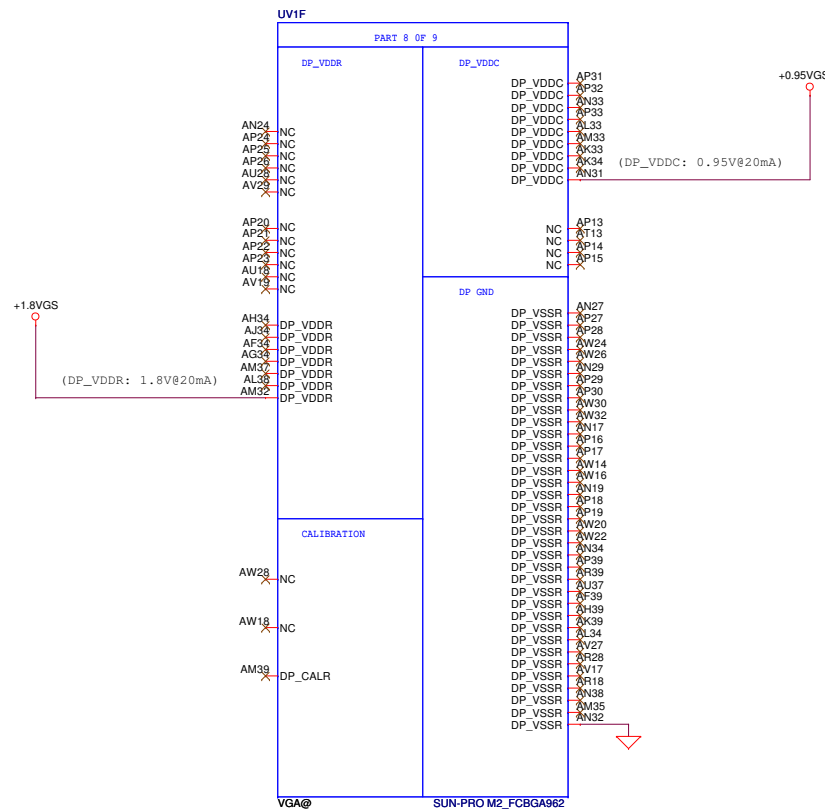
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1



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				LA-9869P
				Rev 0.3
				Date: Wednesday, February 20, 2013 Sheet 14 of 50

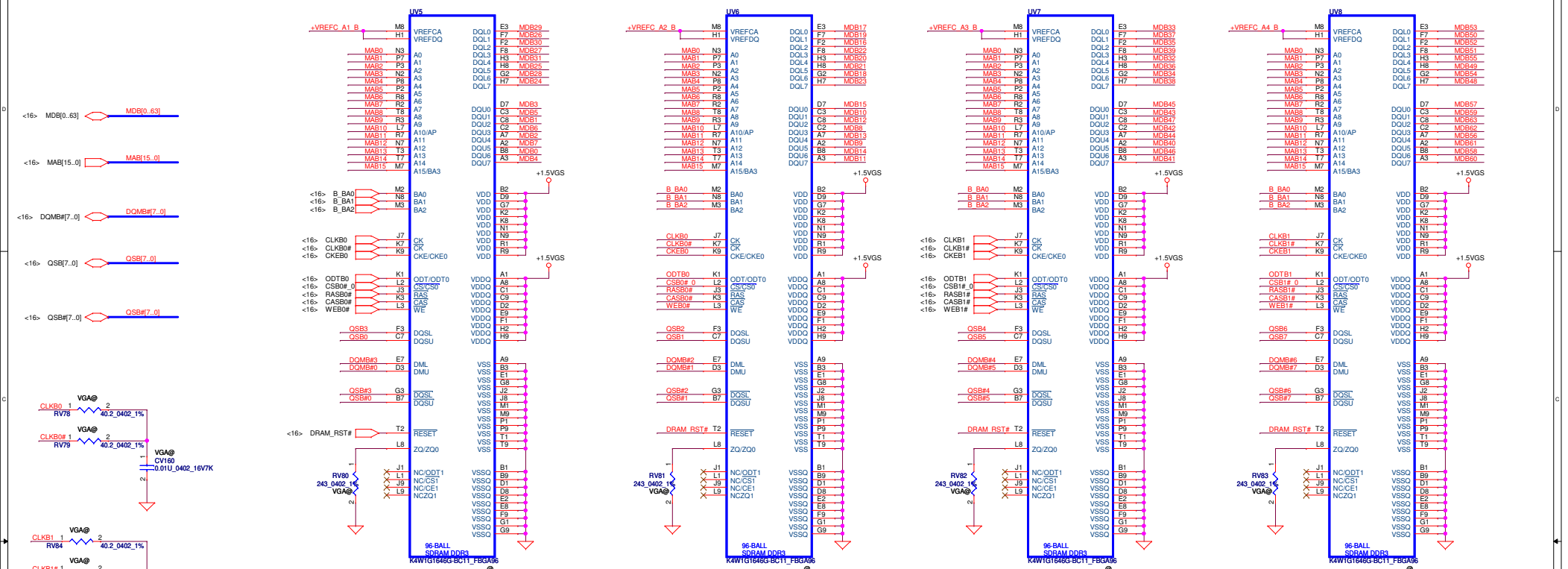


Place all these components close to GPU (Within 25mm)
and keep all component close to each other

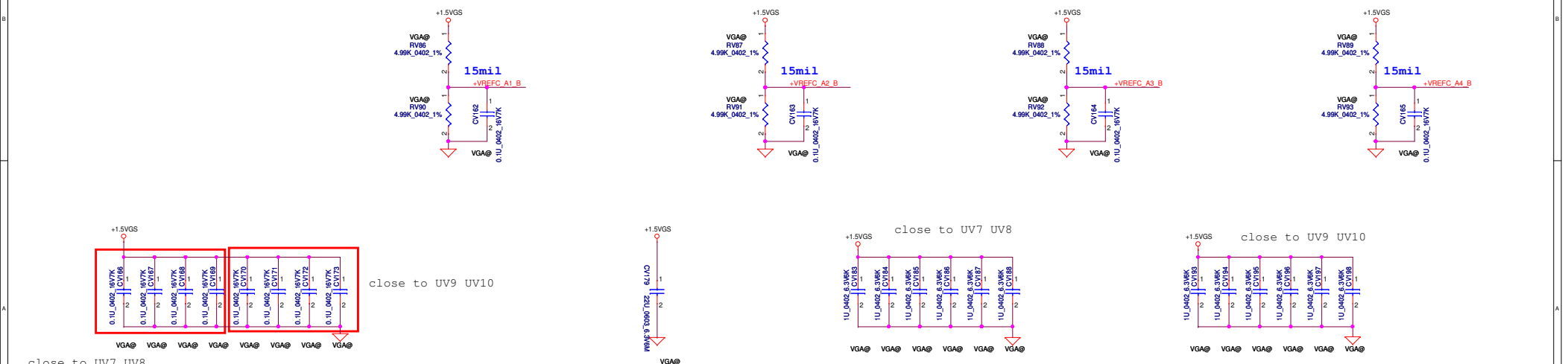


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				LA-9869P	0.3
Date: Wednesday, February 20, 2013				Sheet	17 of 50

CHANNEL B: 512MB/1024MB DDR3



Supported Memory Configurations: Up to 4 Gbit/part for DDR3.

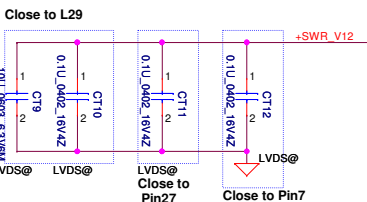
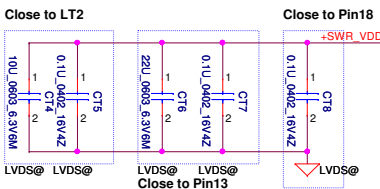
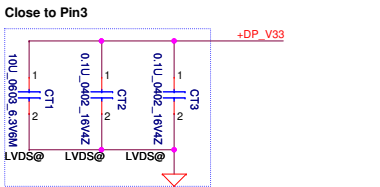
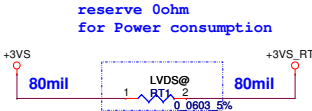


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2013/01/22		2013/01/22		2014/01/21		VRAM Channel B	
Size		Document Number		LA-9869P		Rev	
Date		Wednesday, February 20, 2013		ISheet		18 of 50	

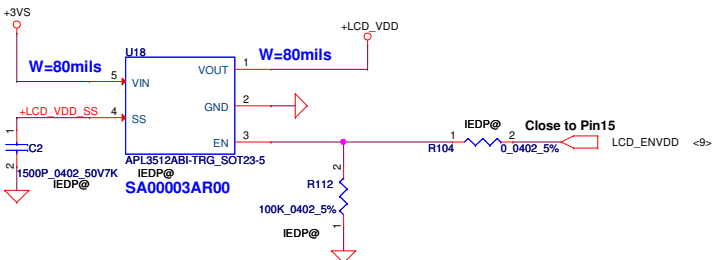
SWR / LDO Mode select		
	LDO	SWR
2132R	RT24	mount LT3

※ If use 2132R, please select LDO mode as default.

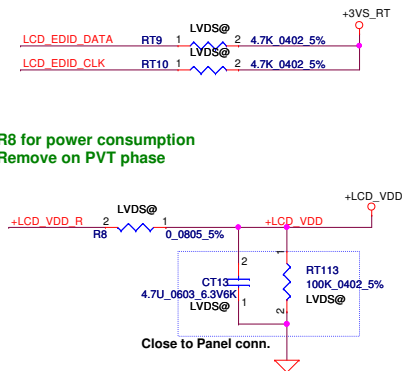
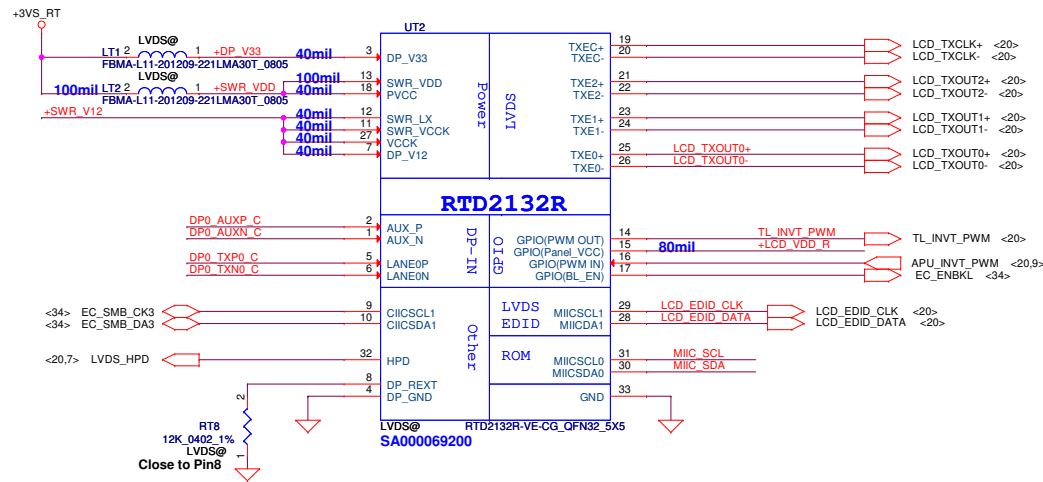
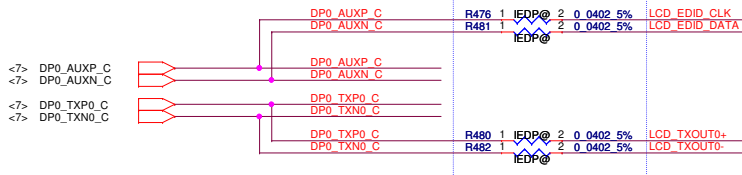
※ If use 2132R, please select LDO mode as default.



LCD POWER CIRCUIT (For eDP panel only)



**R476/481/480/482 need to place under UT2
In order to reduce sub-trace**



R8 for power consumption
Remove on PVT phase

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

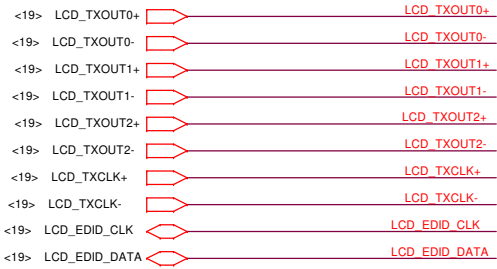
PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V
* Version R has internal level shifter, remove level shifter circuit on AMD platform	

Different between 2132S and 2132R

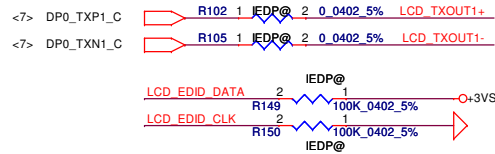
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

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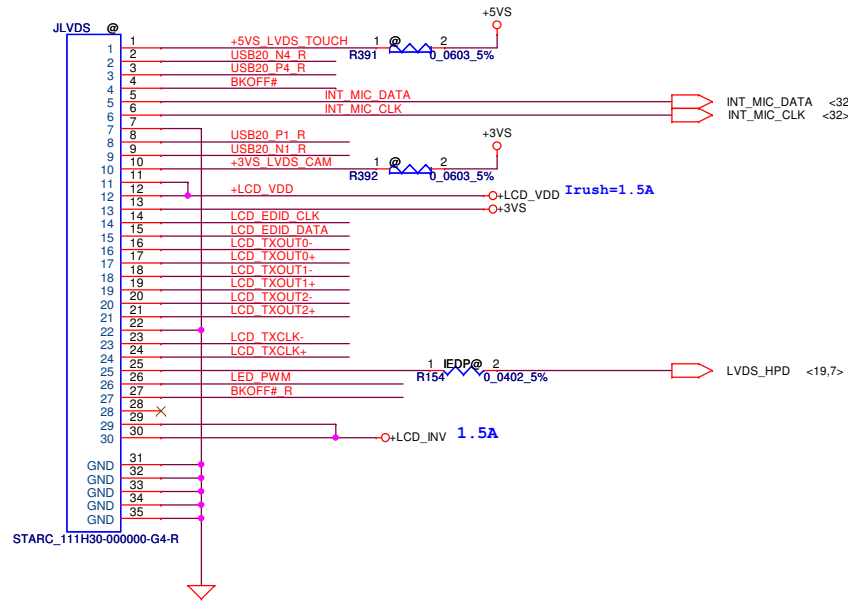
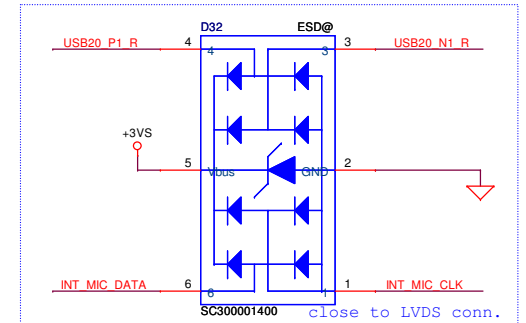
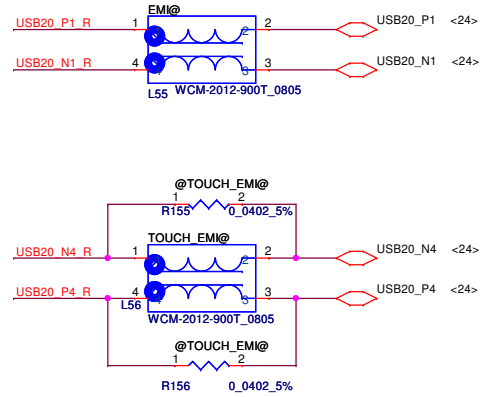
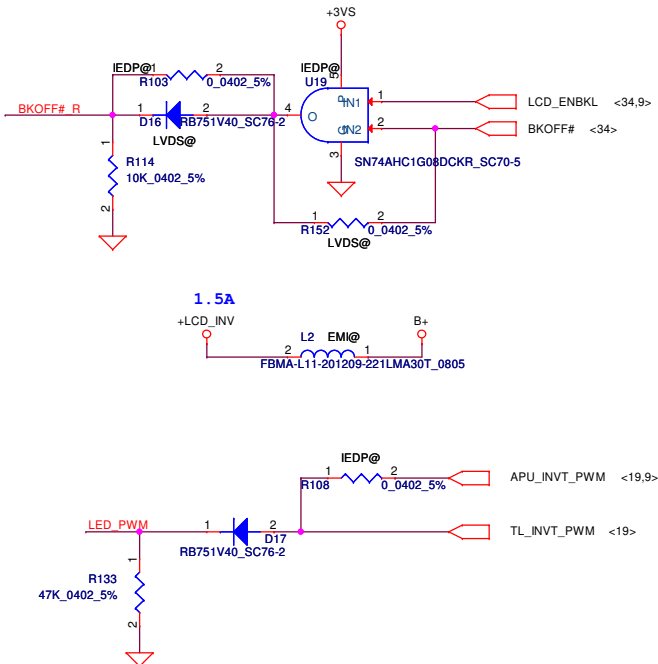
For LVDS 1ch Panel



For eDP Panel

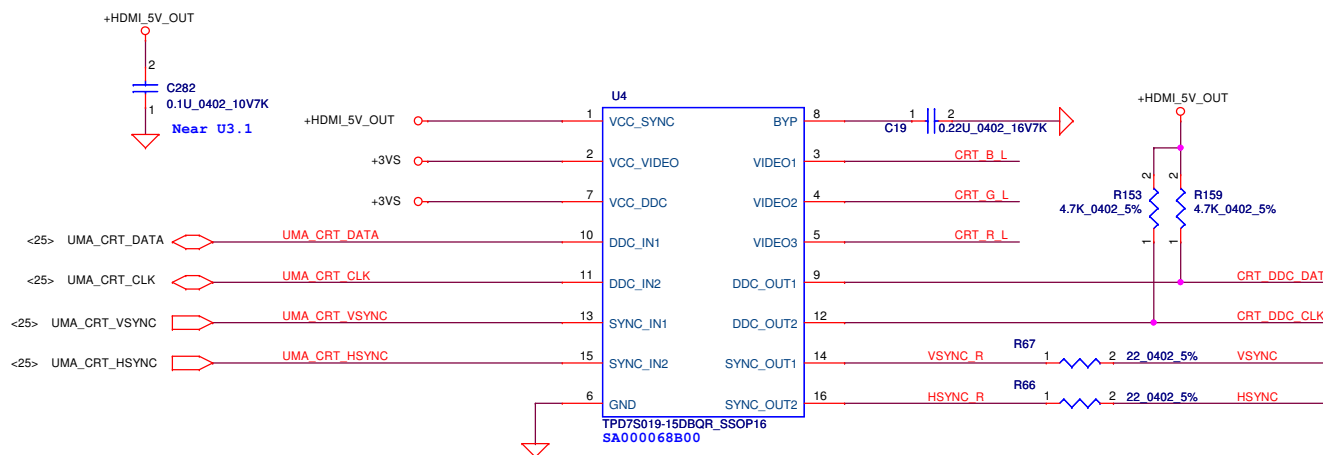
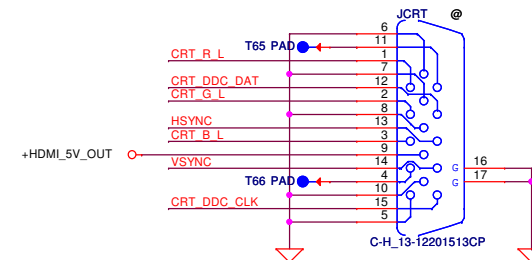
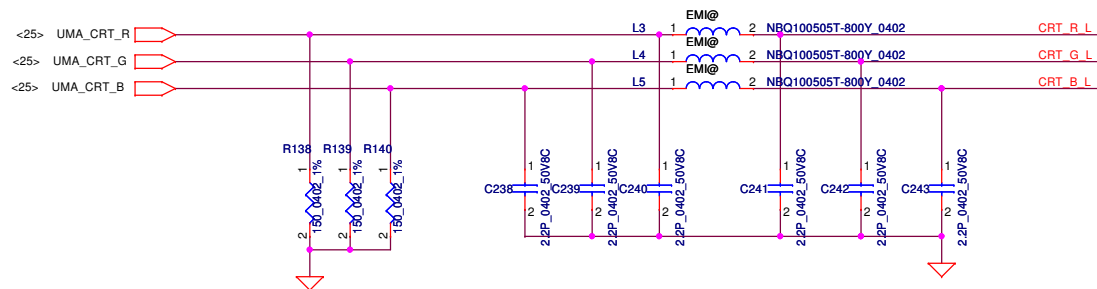


Reserve for eDP panel potience issue



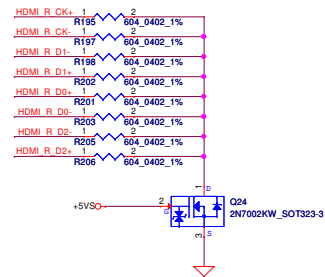
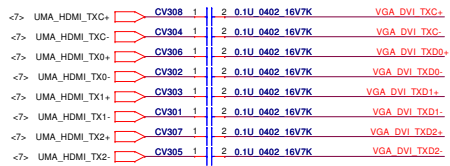
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								LVDS			
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				Sheet	21 of 50
				Rev	0.3

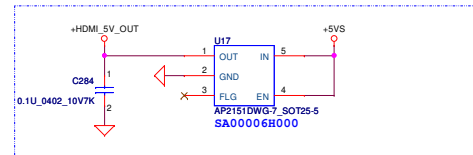
www.vinalix.vn



Change R184 and R185 from 2K to 4.7K for HDMI detect issue on Comal

HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A, RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



HDMI Royalty

ZZZ HDMI45@

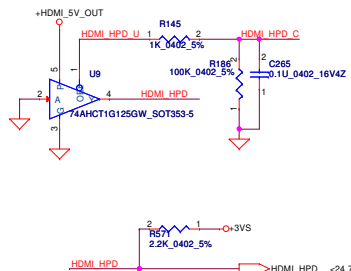
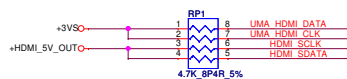
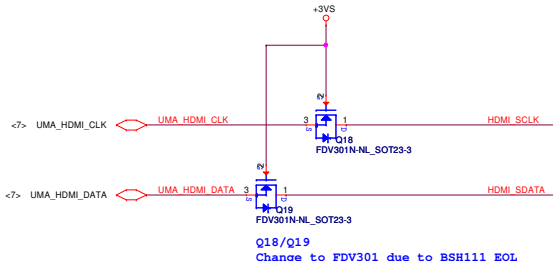
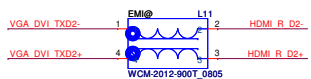
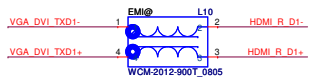
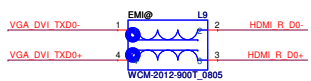
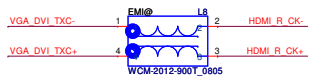
RO0000003HM

HDMI W/Logo + HDCP

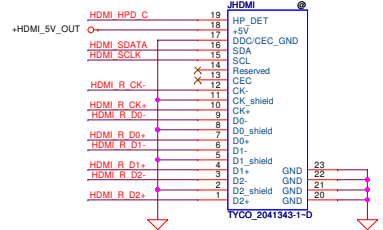
HDMI W/O Logo: RO0000001HM

HDMI W/Logo: RO0000002HM

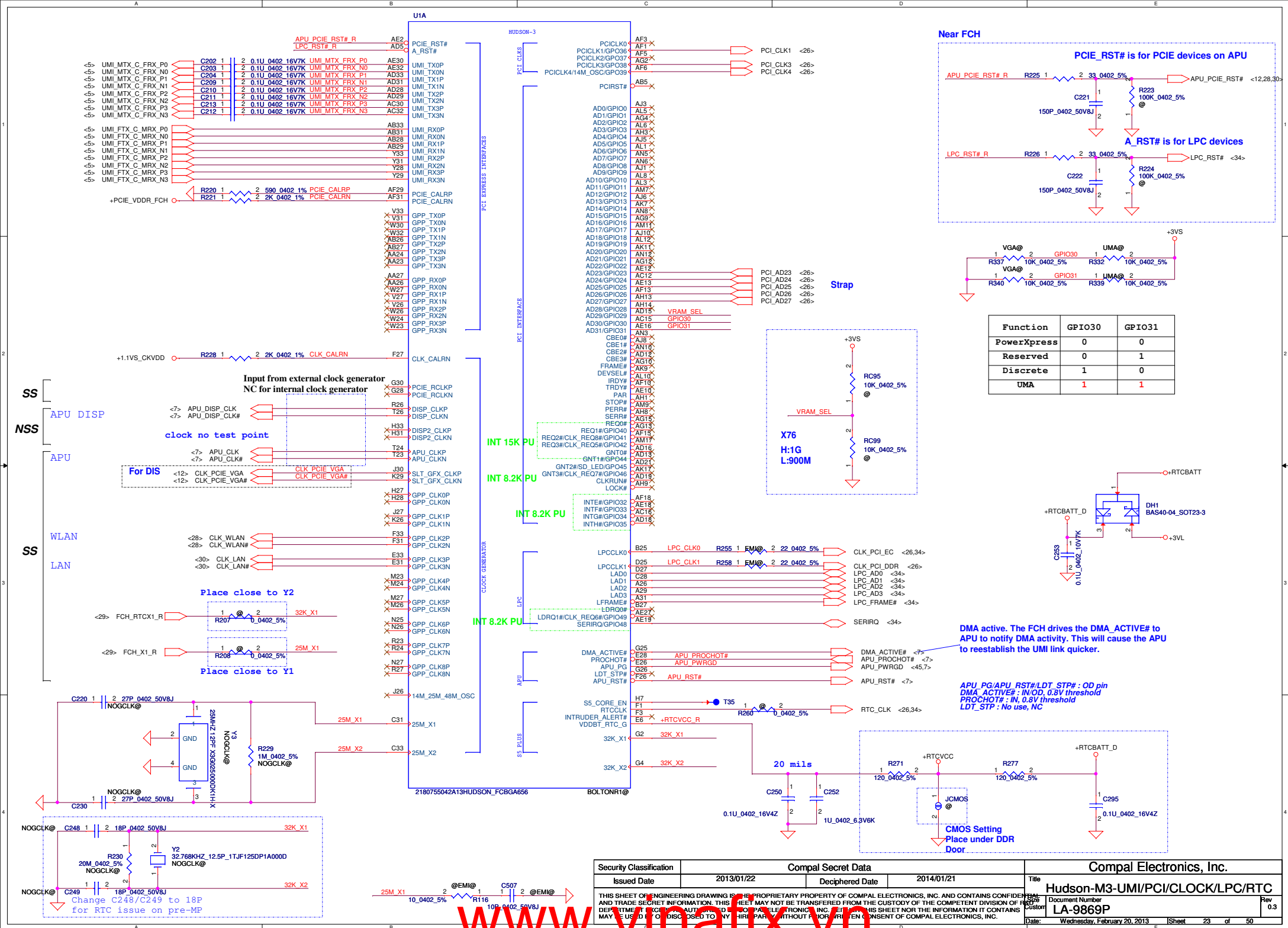
HDMI W/Logo + HDCP: RO0000003HM



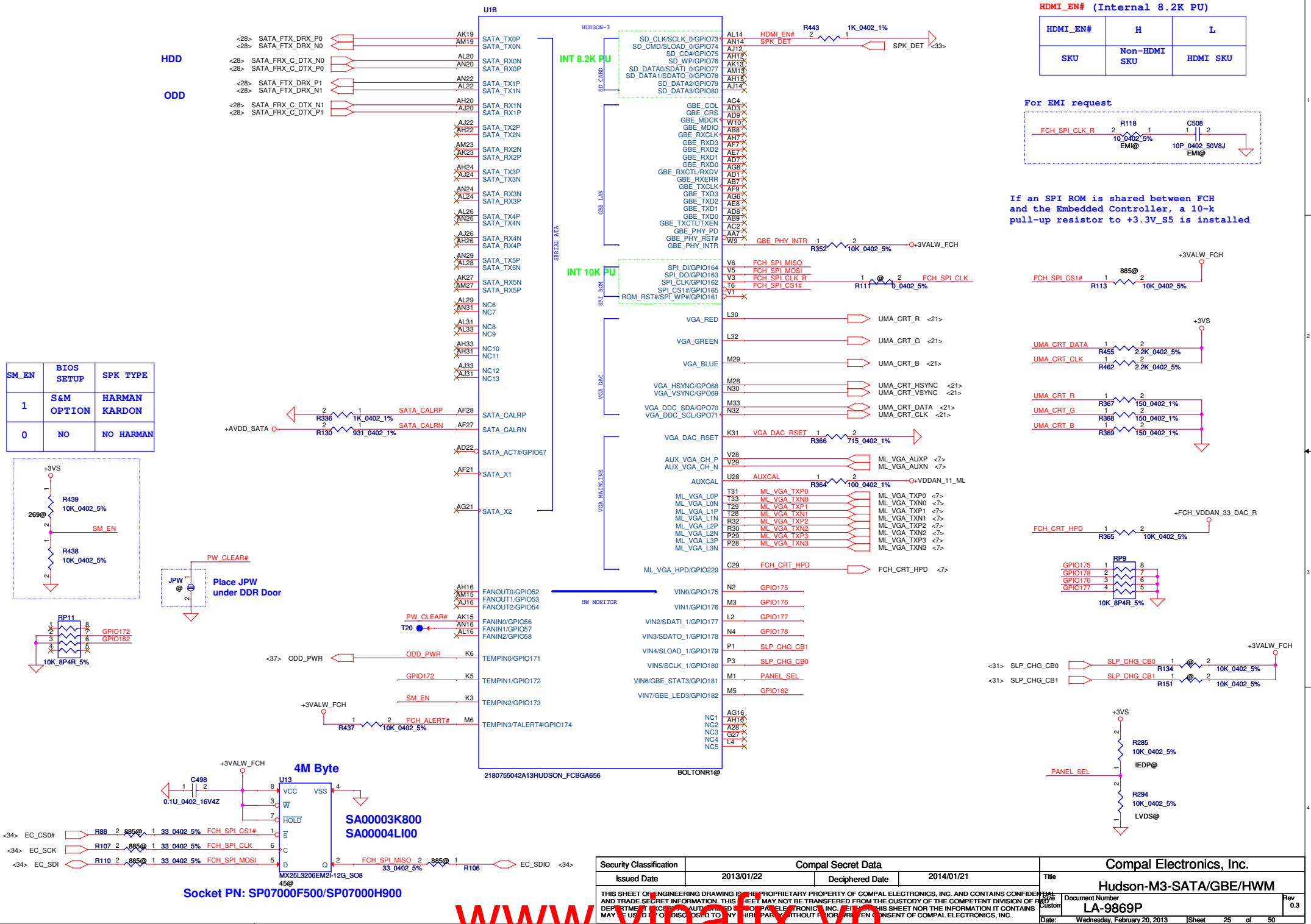
HDMI Connector



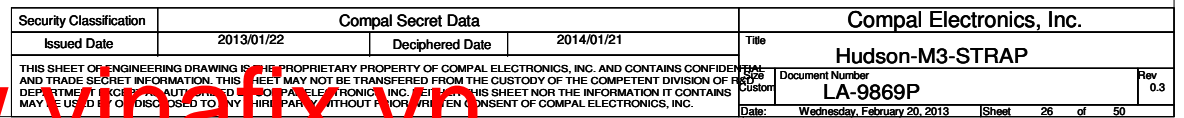
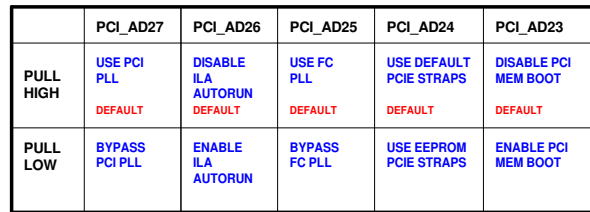
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Issued Date	2013/01/22	Deciphered Date	2014/01/21	HDMI Conn./CEC	
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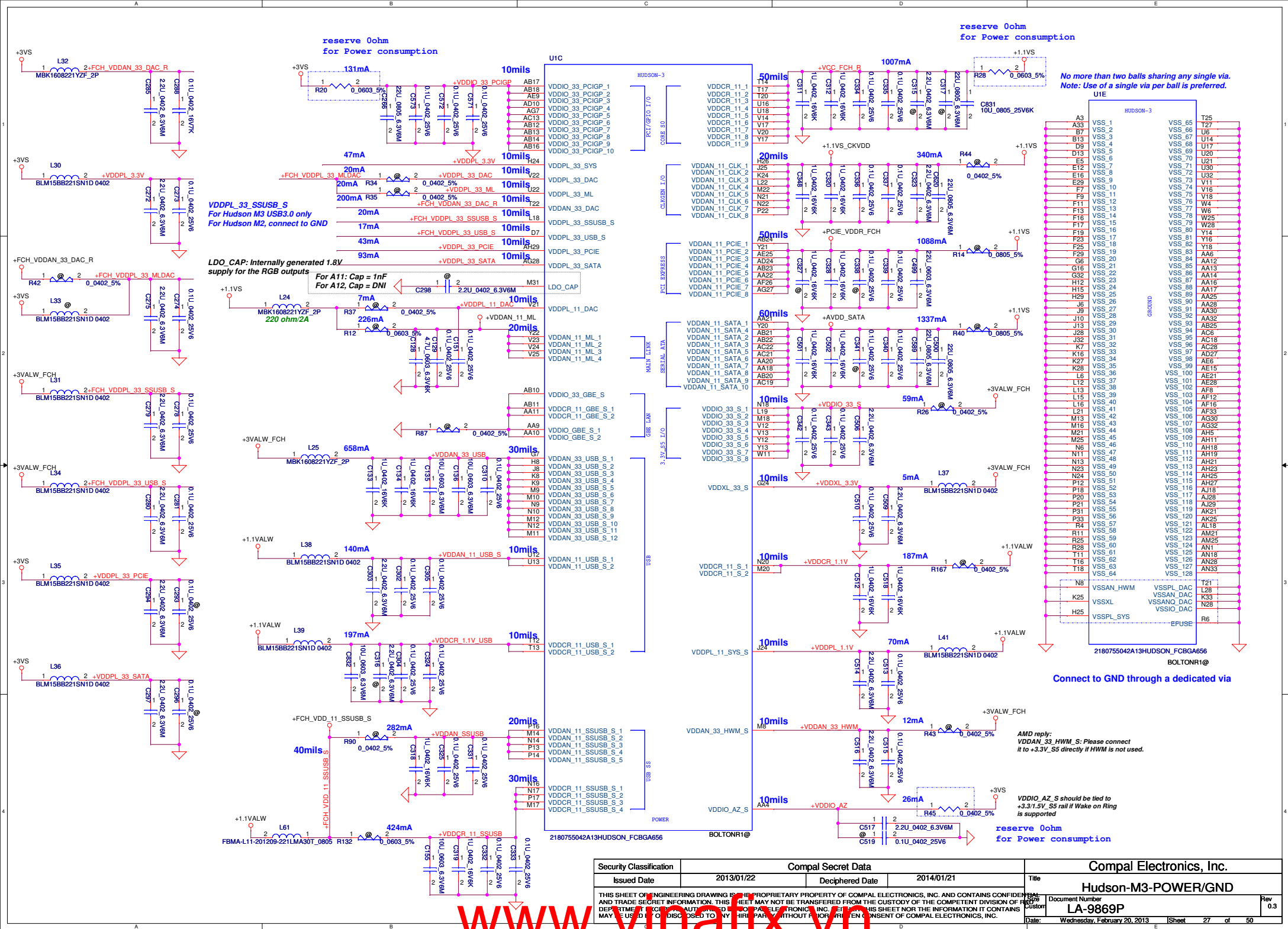




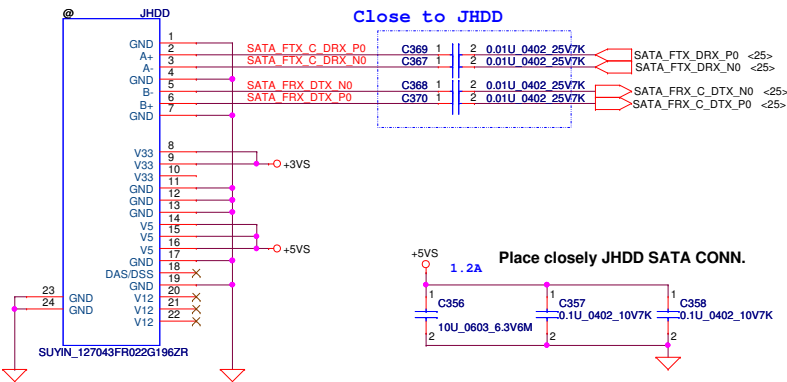


	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

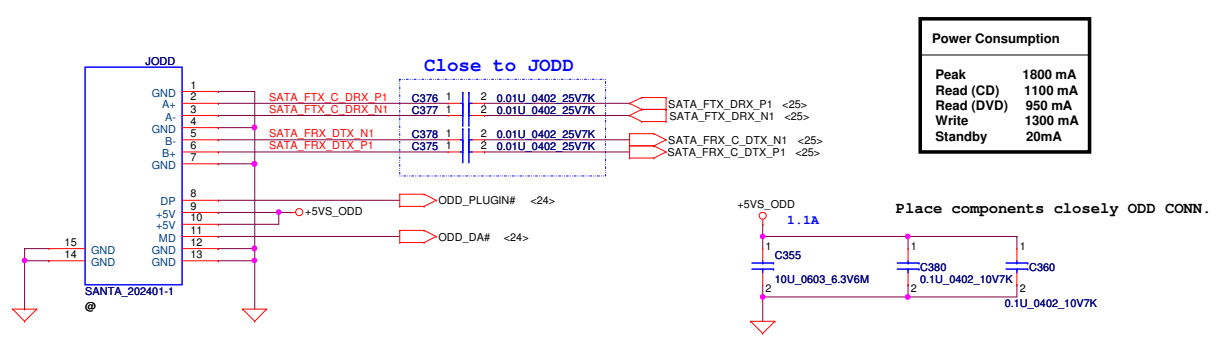




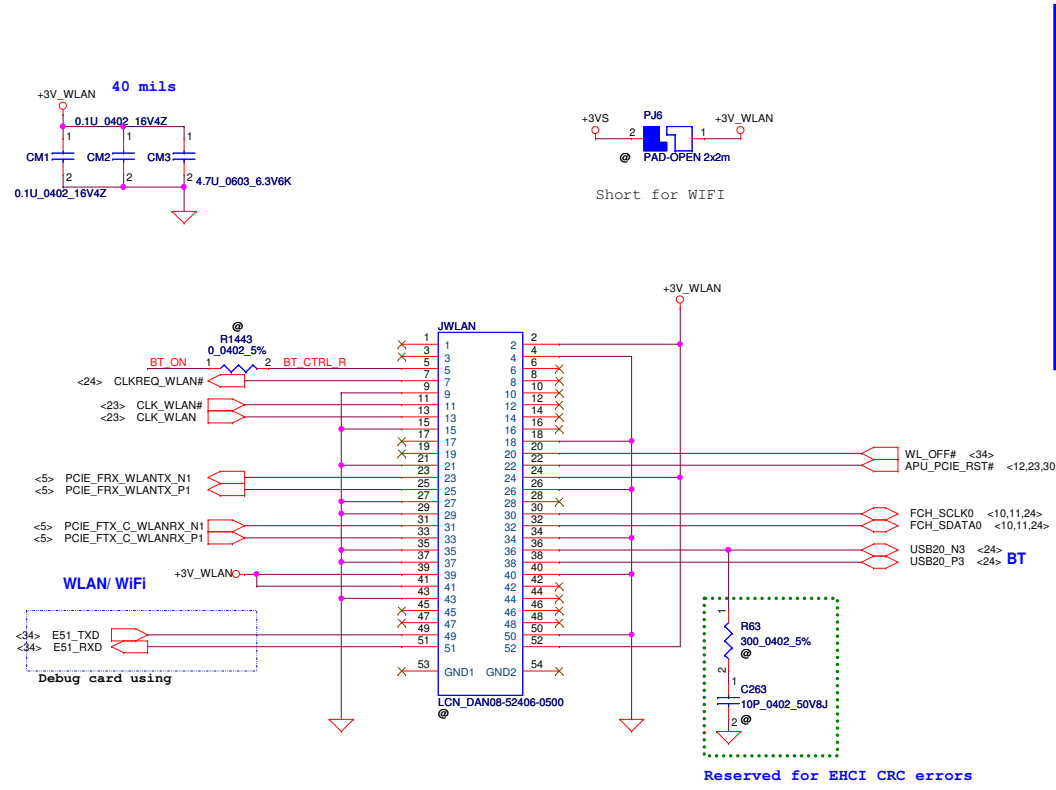
SATA HDD Conn.



SATA ODD Conn



Slot 1 Half PCIe Mini Card-WLAN

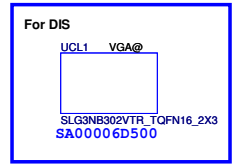


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

For isolate BT_CTRL and Compal Debug Card.

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

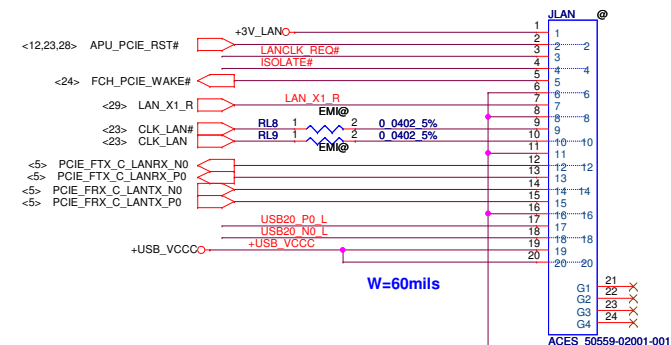
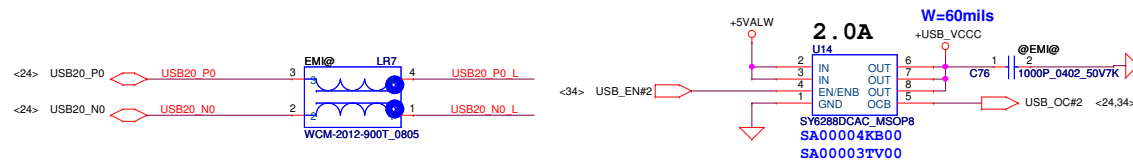


The diagram shows a timing relationship for the GCLK module. A pink oval highlights the core logic, which is a block labeled 'YCL1' with the part number '29MHZ 12PF X3G025000DK1H-X'. The block has two inputs: 'CLK_X1' (pin 1) and 'CLK_X2' (pin 3). It has two outputs: 'GCLK@' (pin 2) and 'GCLK@' (pin 4). The 'GCLK@' signal is shown as a square wave. The 'CLK_X1' and 'CLK_X2' signals are shown as square waves. The 'GCLK@' signal is derived from 'CLK_X1' and 'CLK_X2'.

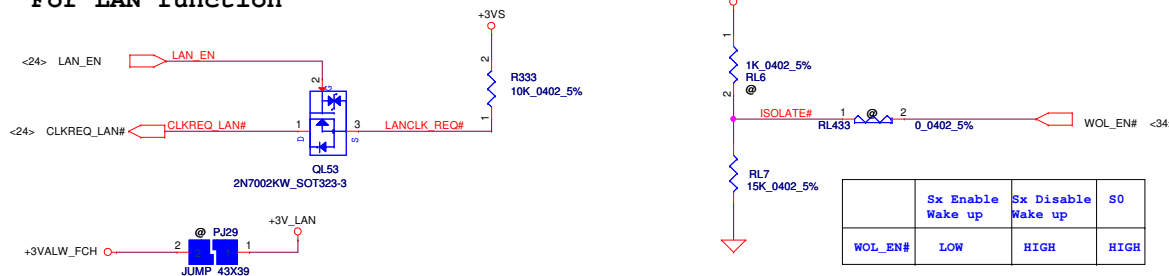
LAN_X1_R_R 1 @ 2 CCL10 5P_0402_50V8C

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Left USB 2.0 x 1



For LAN function

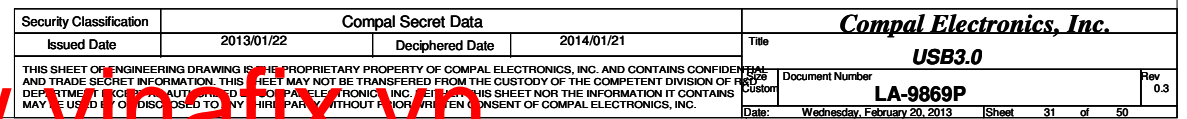
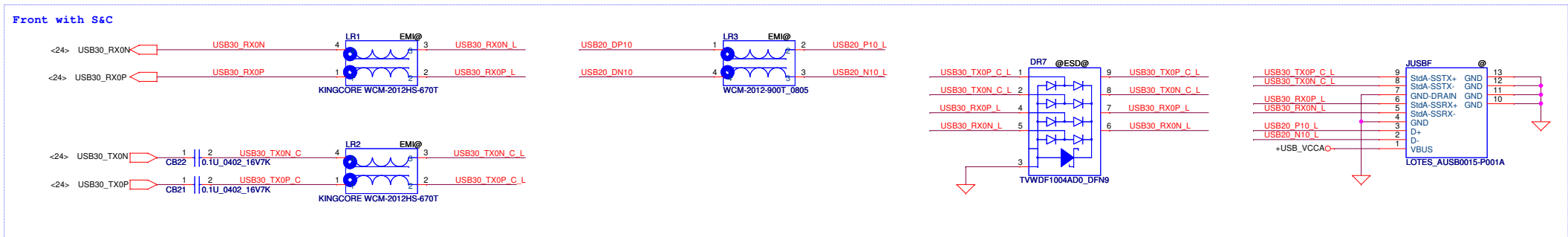


+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

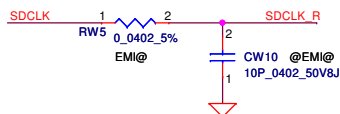
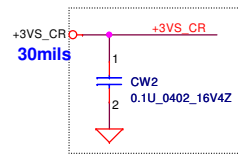
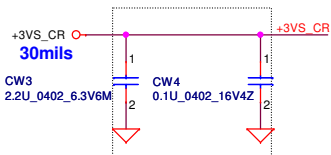
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.



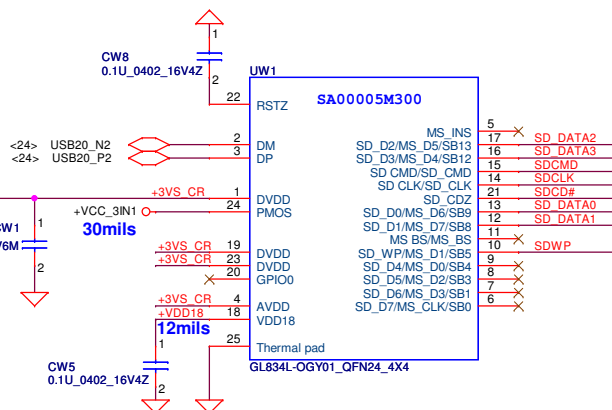
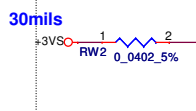
Card reader

please close the pin4 of UW1

please close the pin19 of UW1



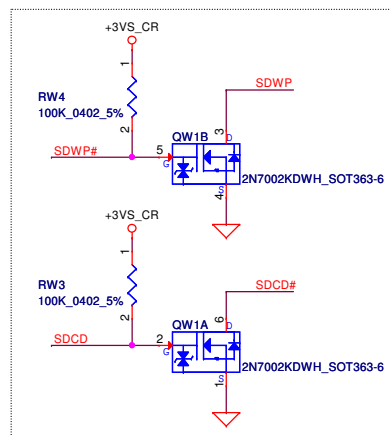
For power consumption measurement and remove it after Pre-MP phase



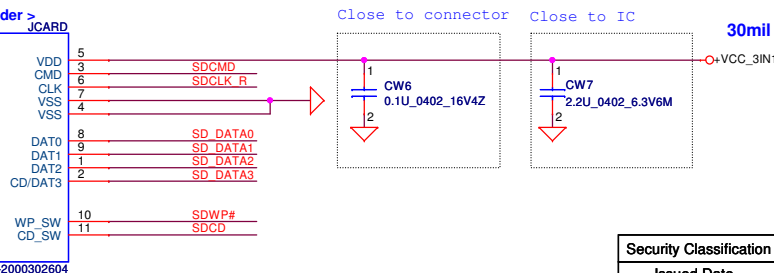
	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

	CD_SW	WP_SW	
Card Uninsertion	Close	Protect disable	Protect Enable
		Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit



< 2 in 1 Card Reader >

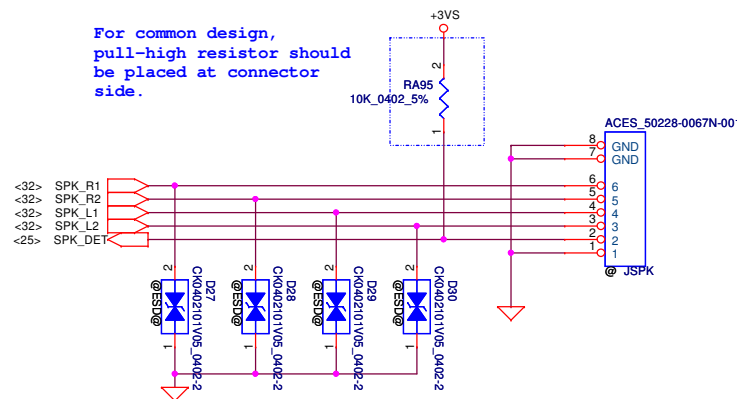


"Normal Close" type connector

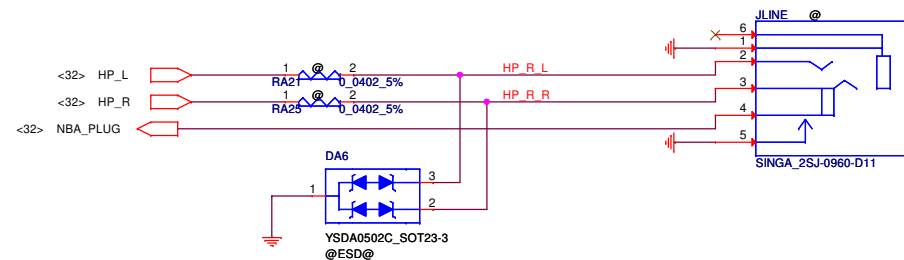
SPK CONN.

	Non-Harman detection	
SPK_DET0	0	ONKYO
	1	Non-Brand

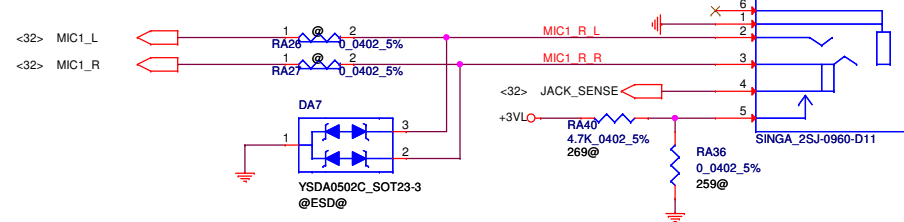
Please check SPK DET pull high 10K to +3VS



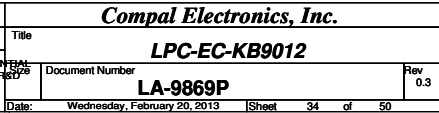
HeadPhone/LINE Out JACK



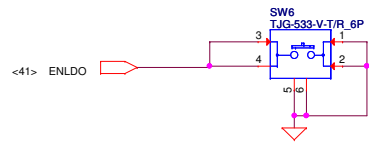
Ext.MIC/LINE IN JACK



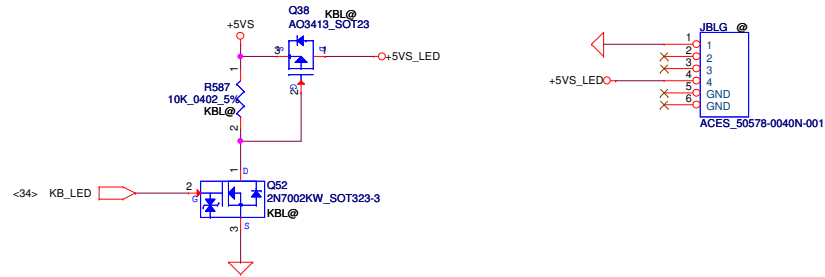
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/01/22	Deciphered Date	2014/01/21	Title		
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				Size	Document Number	Rev
					LA-9869P	0.5
Date:				Wednesday, February 20, 2013	ISheet	33 of 50



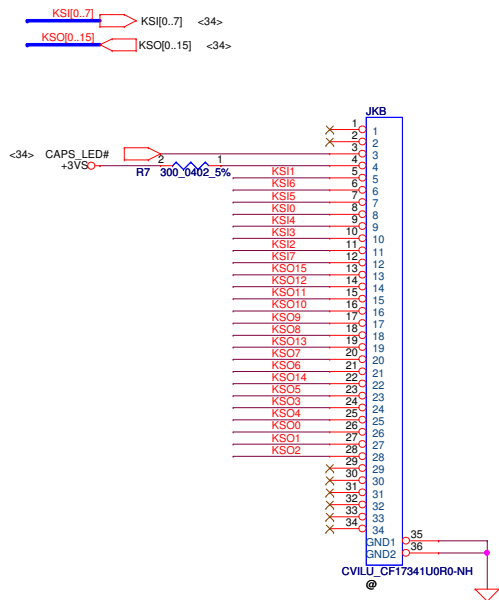
Battery Reset



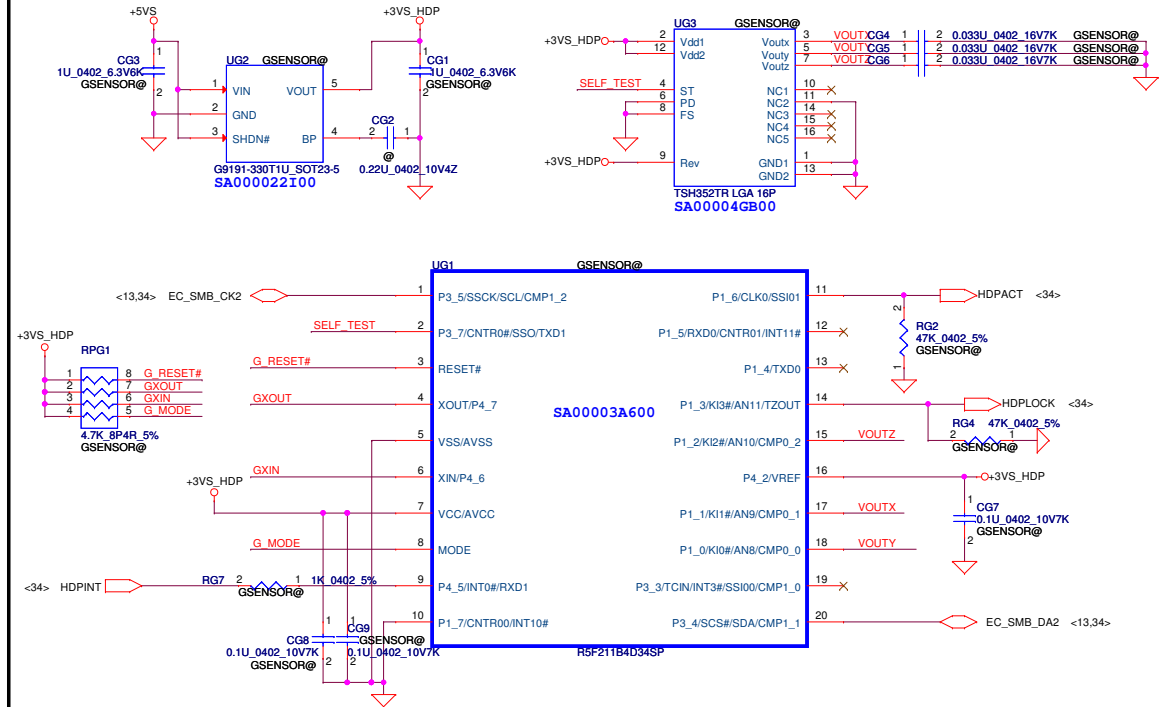
Keyboard LED



NEW KEYBOARD CONN.

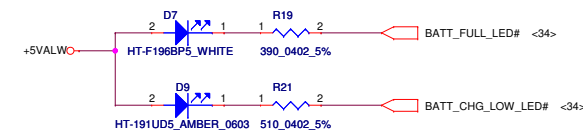


G-SENSOR



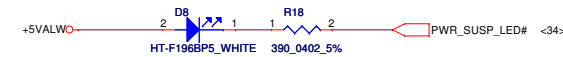
LED

BATT CHARGE (Blink) /FULL LED



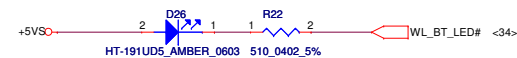
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED (Blink)



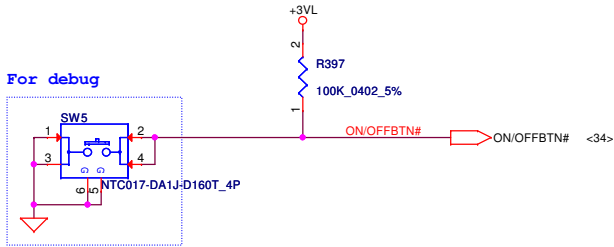
White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN LED

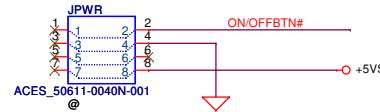


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/01/22	Deciphered Date	2014/01/21	Title
				Debug/KB
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				LA-9869P
				Rev 0.3
				Date: Wednesday, February 20, 2013 Sheet 35 of 50

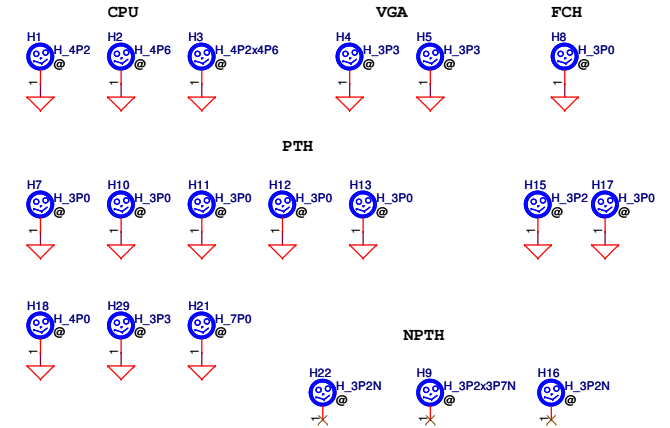
For debug
Place on TOP



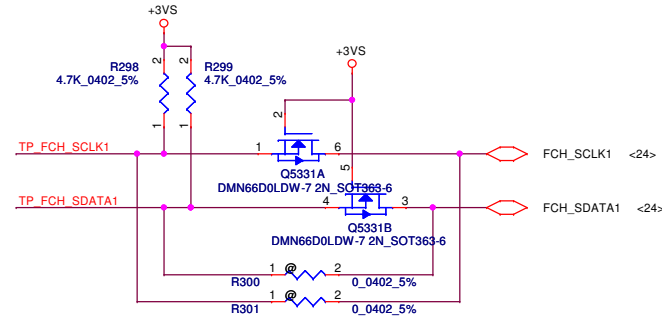
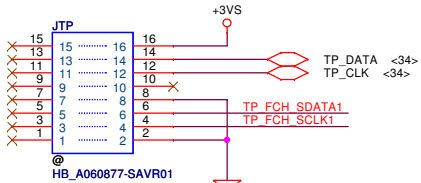
Conn.



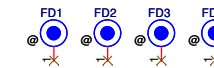
Screw Hole



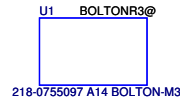
Touchpad Connector



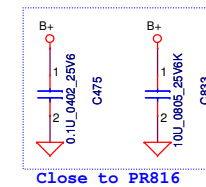
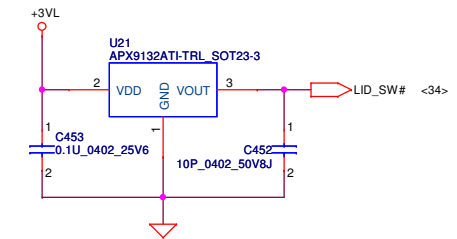
PCB Fedical Mark PAD



ISPD

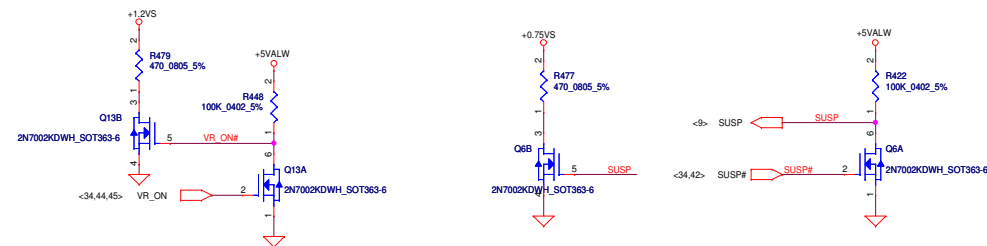
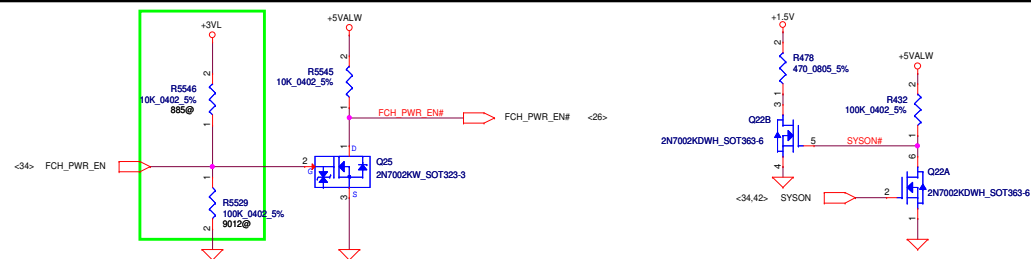
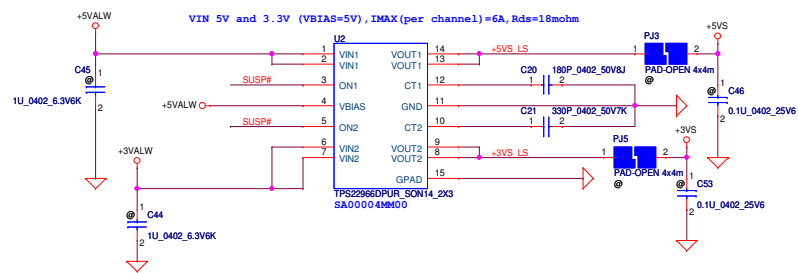


Lid SW

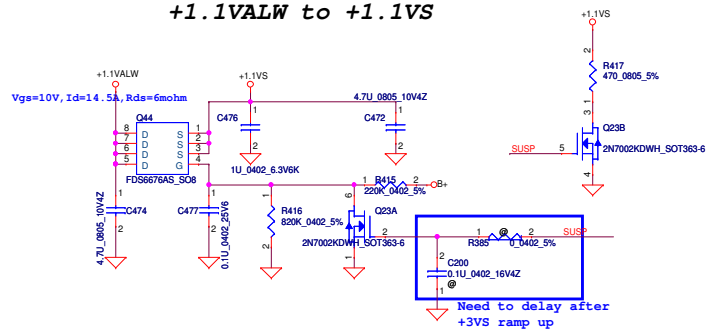


Security Classification		Compal Secret Data				
Issued Date	2013/01/22	Deciphered Date	2014/01/21	Title		
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				Size	Document Number	Rev
				LA-9869P		0.3
				Date: Wednesday, February 20, 2013		
				Sheet 36 of 50		

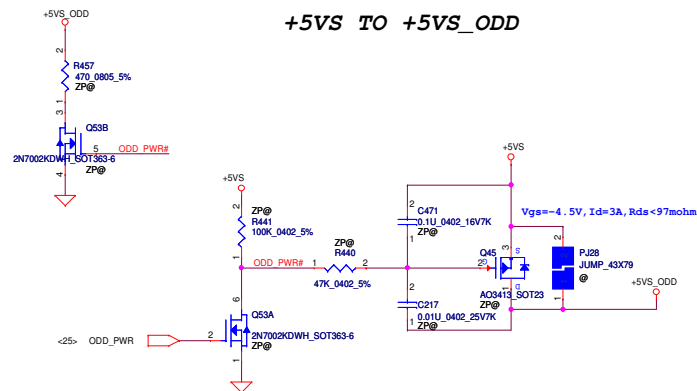
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



+1.1VALW to +1.1VS



+5VS TO +5VS_ODD

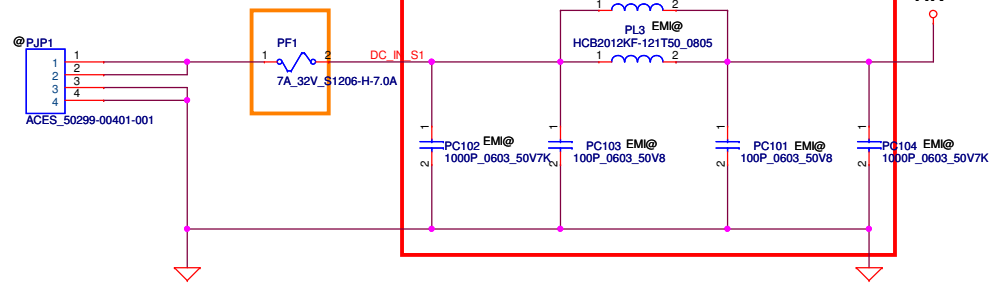


Security Classification		Compal Secret Data		Compal Electronics, Inc. DC-DC INTERFACE		
Issued Date	2013/01/22	Deciphered Date	2014/01/21	Title		
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				LA-9869P Date: Wednesday, February 20, 2013 Sheet 37 of 50		
				0.3		

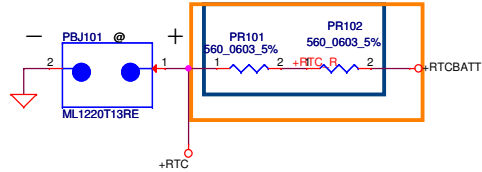
EMI Part (47.1)

Other component (37.1)

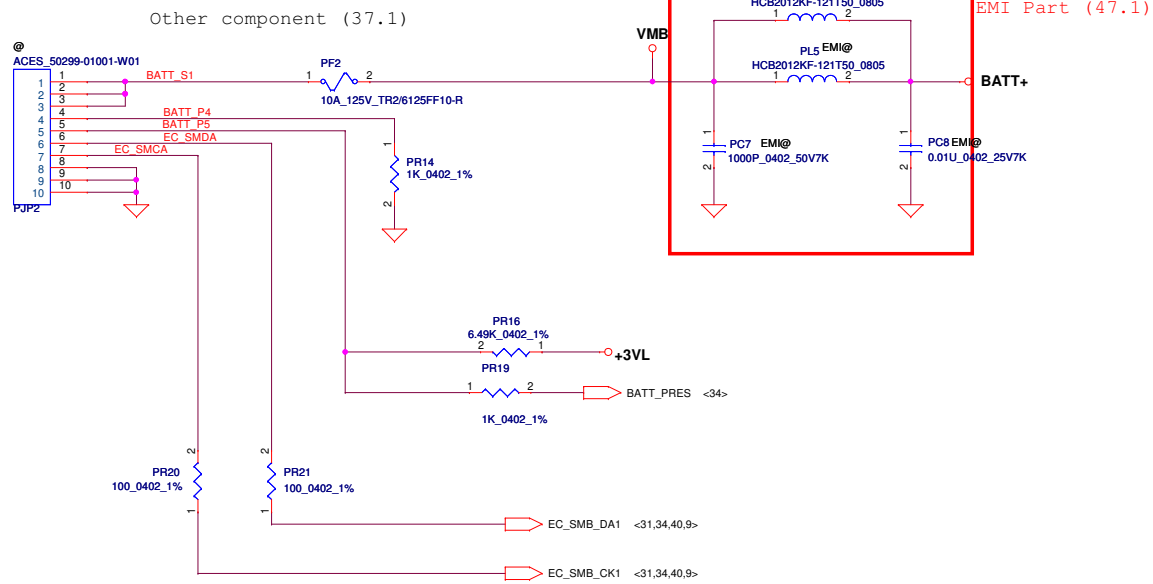
A51 need add fuse



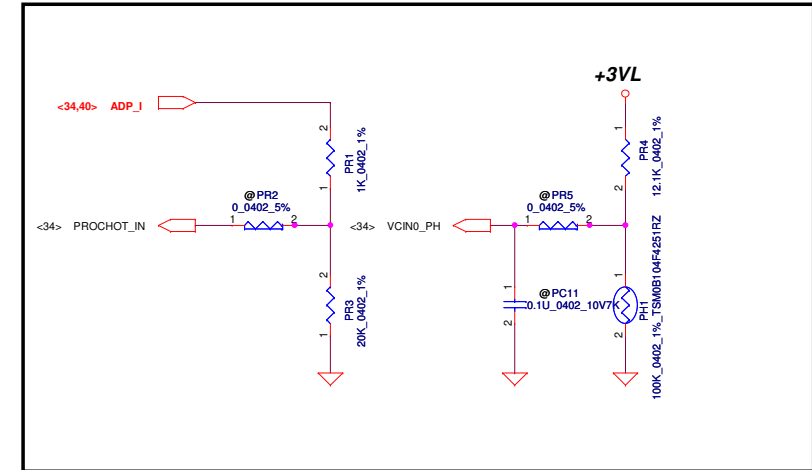
For ML1220 RTC (38.2)



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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title
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				Custom
				LA-9869P
				Rev 0.1
				Date:
				Sheet 38 of 49



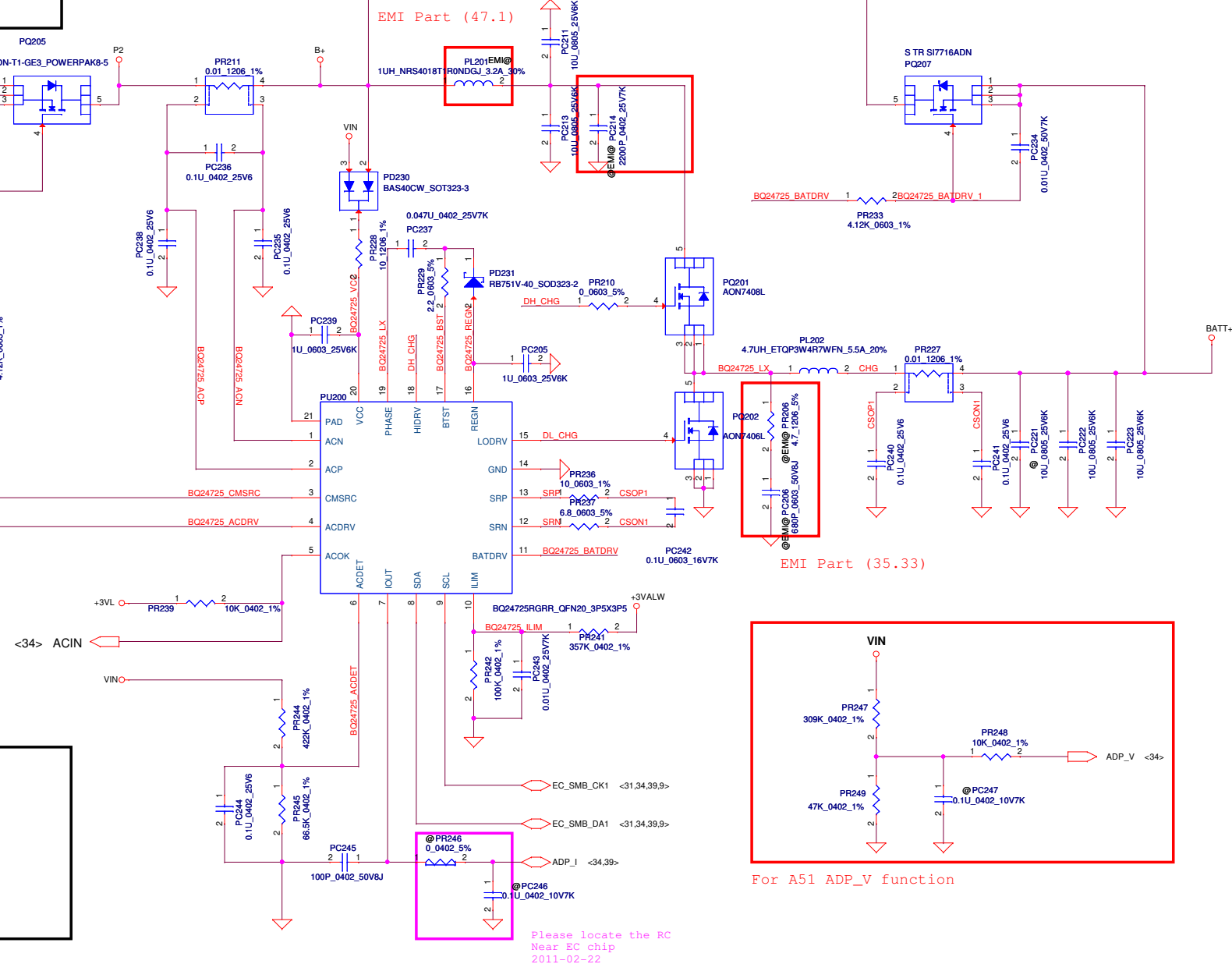
OTP (39.7)



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	BATTERY CONN / OTP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Custom
				Document Number	LA-9869P
				Date:	Sheet 39 of 49

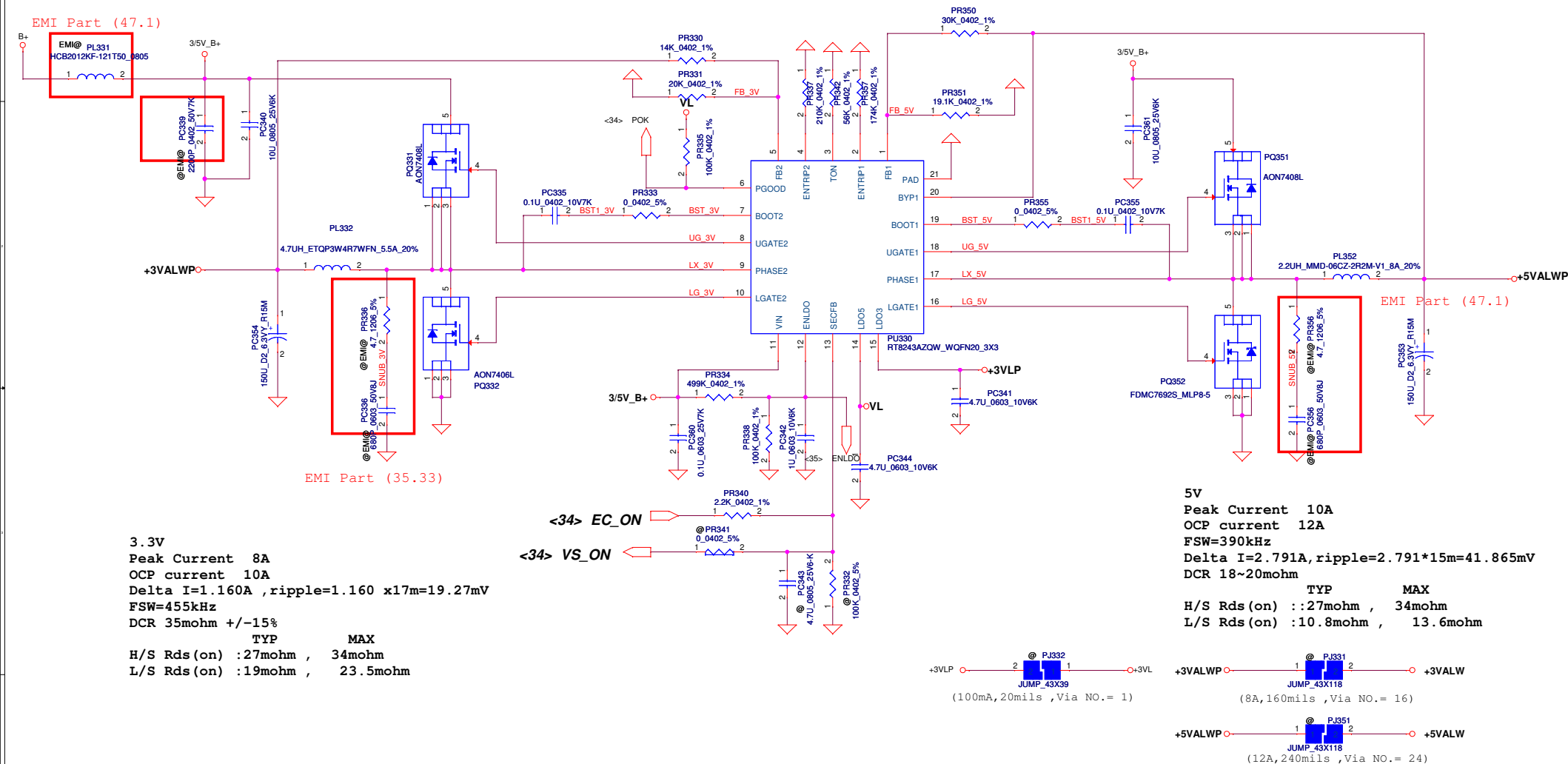
for reverse input protection

Charger controller (40.1), Support component (40.2)

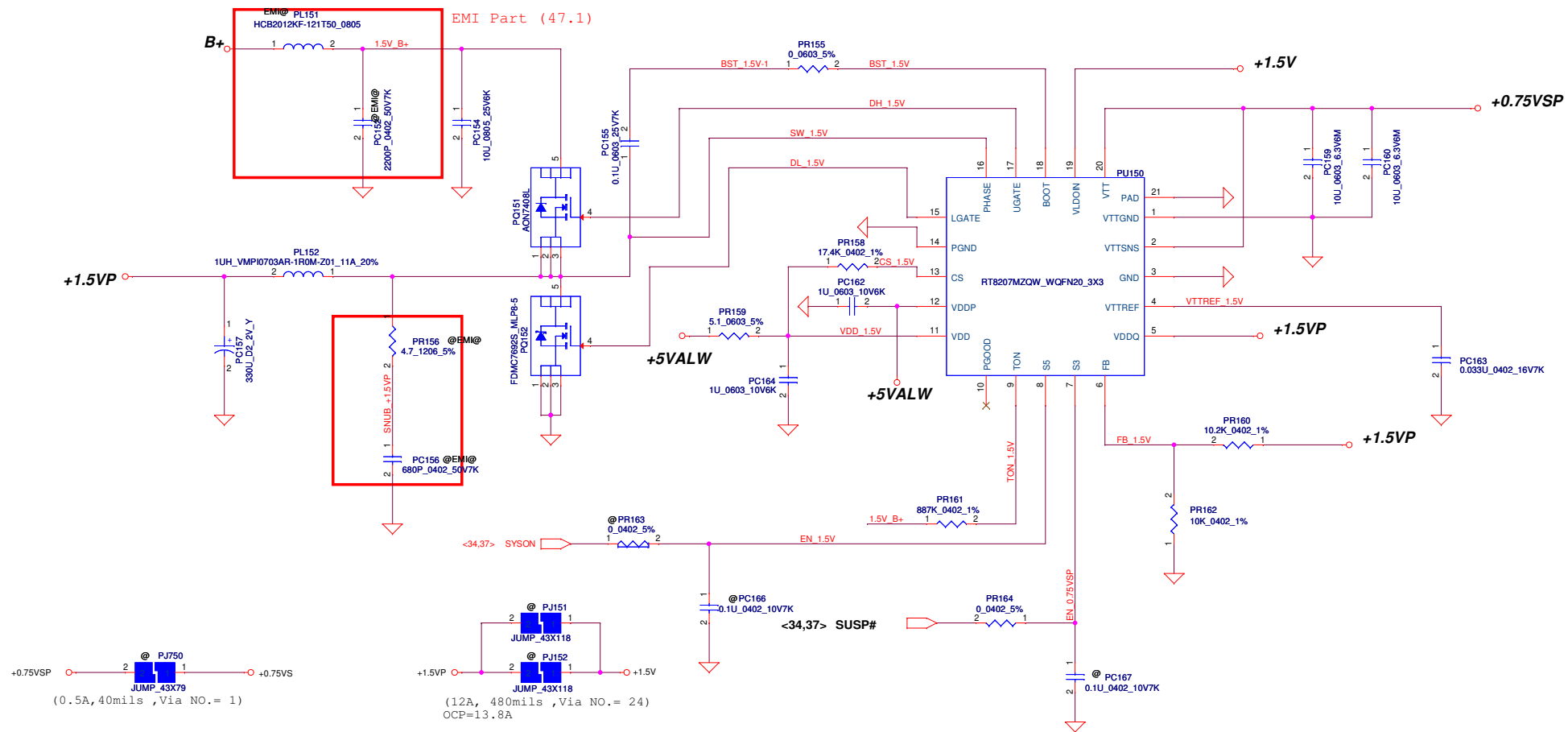


Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
3.97A			

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	CHARGER
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				Custom	Rev 0.1
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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	3VALW/5VALW
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				Sheet	41 of 49



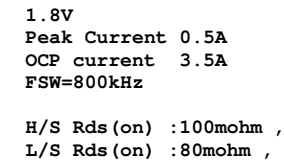
1.5V
Peak Current 12A
OCP current 13.34A
FSW=300kHz
DCR 8.3 ~ 10mohm
TYP MAX
H/S Rds (on) : 27mohm , 34mohm
L/S Rds (on) : 10.8mohm , 13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

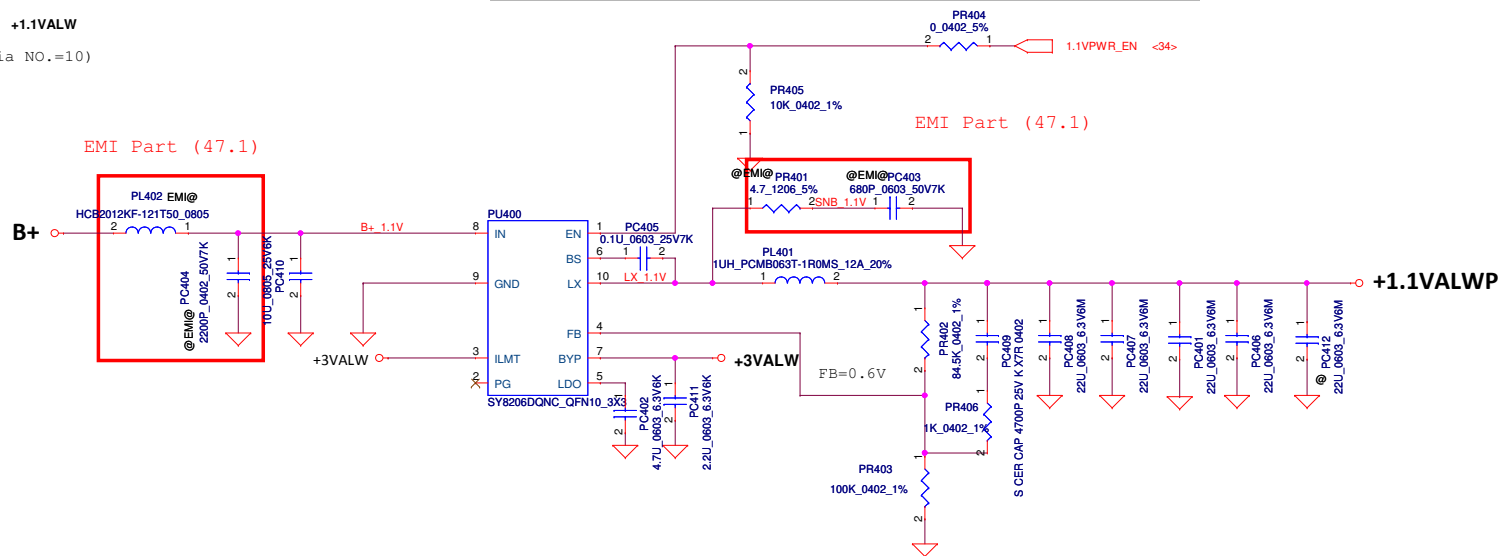
Note: S3 - sleep ; S5 - power off

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title		
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				Size	Document Number	Rev
				Custom	LA-9869P	0.1
Date:				Sheet 42 of 49		

```
1.8V controller (35.15), Support component (35.16)
```



```
1.1V controller (35.27), Support component (35.28)
```



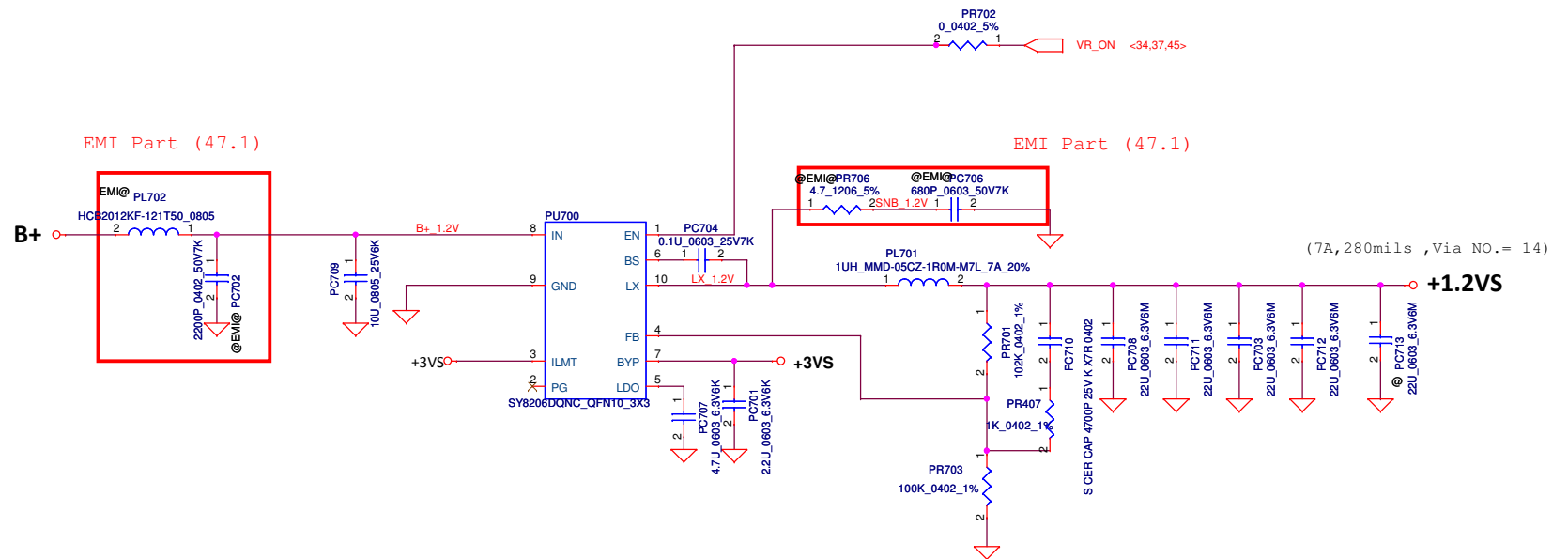
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/06	Deciphered Date	2015/09/06	Title	+1.8VALWP
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				Custom	LA-9869P
				Date:	Wednesday, February 20, 2013
				Sheet	43 of 49
				Rev	0.1

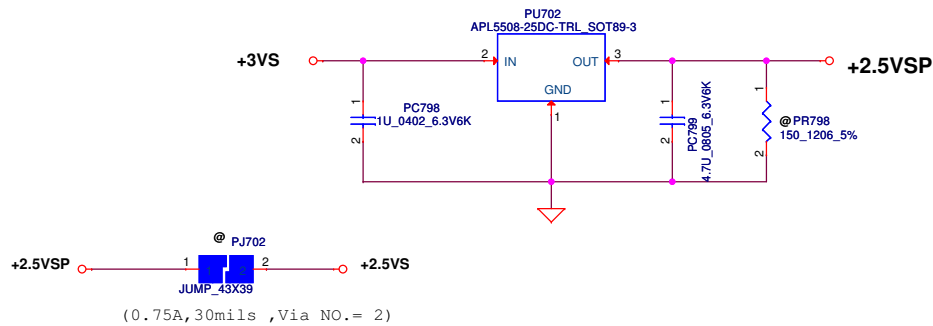
1.2V controller (35.7), Support component (35.8)

1.2V
Peak Current 7A
OCP current 12A
FSW=800kHz

H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,



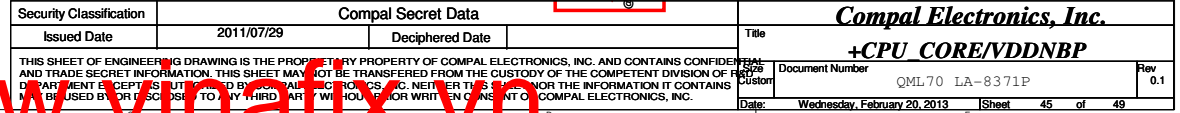
2.5V controller (35.13), Support component (35.14)



Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2012/09/06		Deciphered Date		2015/09/06	
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				+1.2VSP/+2.5VSP			
				Size		Document Number	
		Custom		LA-9869P		0.1	
Date:		Wednesday, February 20, 2013		Sheet		44 of 49	

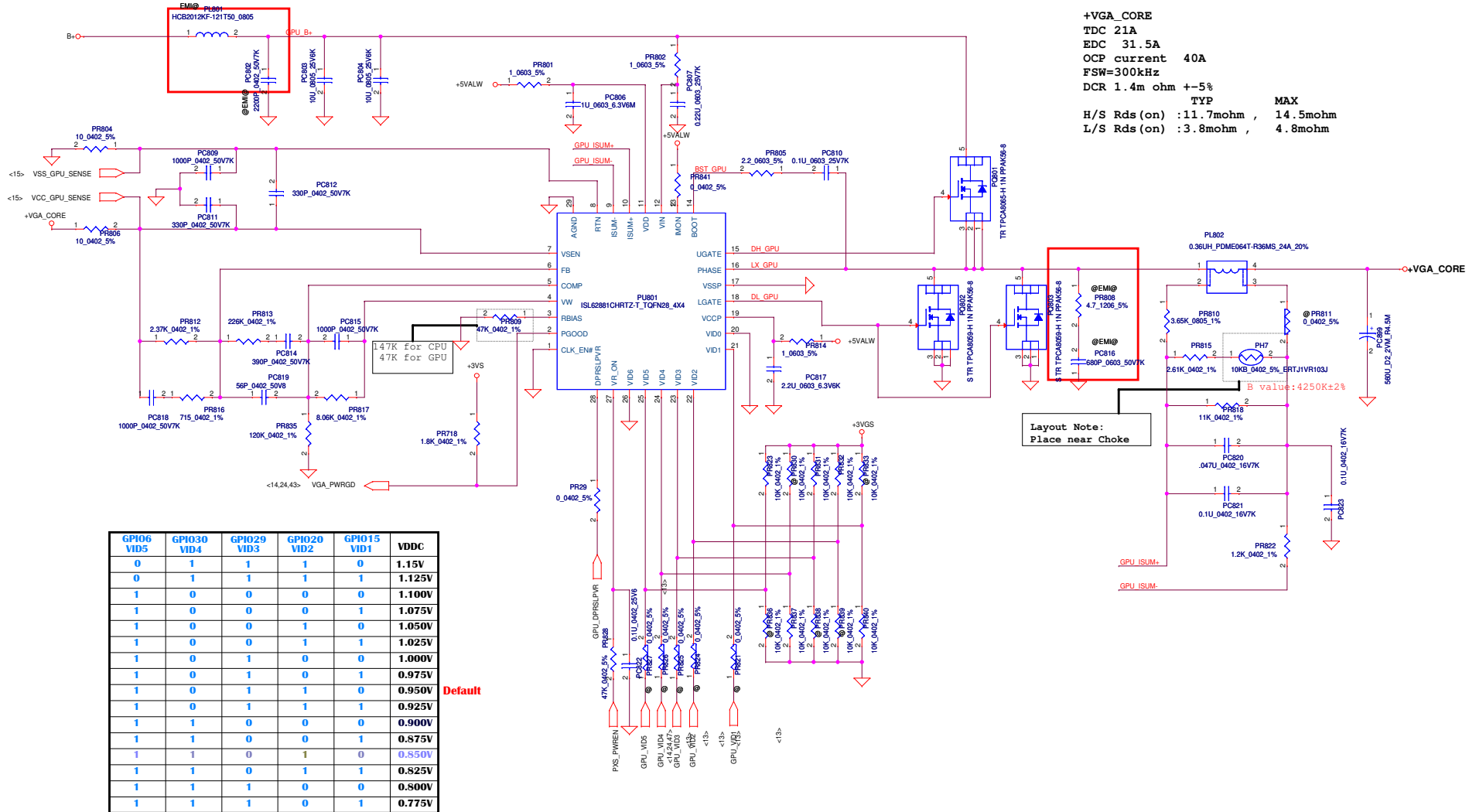
CPU controller (36.1), Driver (36.2) Support component (36.3)

+APU_CORE_NB		LOATE1
TDC (AB) 22A	(C) 30A	
EDC (AB) 33A	(C) 40A	
OCP current (AB) 41.51A		
Load line -4mV/A		
FSW=450kHz		
DCR 1mohm ~1.2mohm		
	TYP	MAX
H/S Rds(on)	: 7.4mohm ,	8.8mohm
L/S Rds(on)	: 2.6mohm ,	3.1mohm

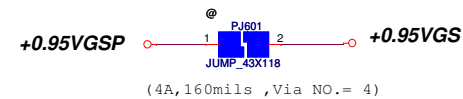
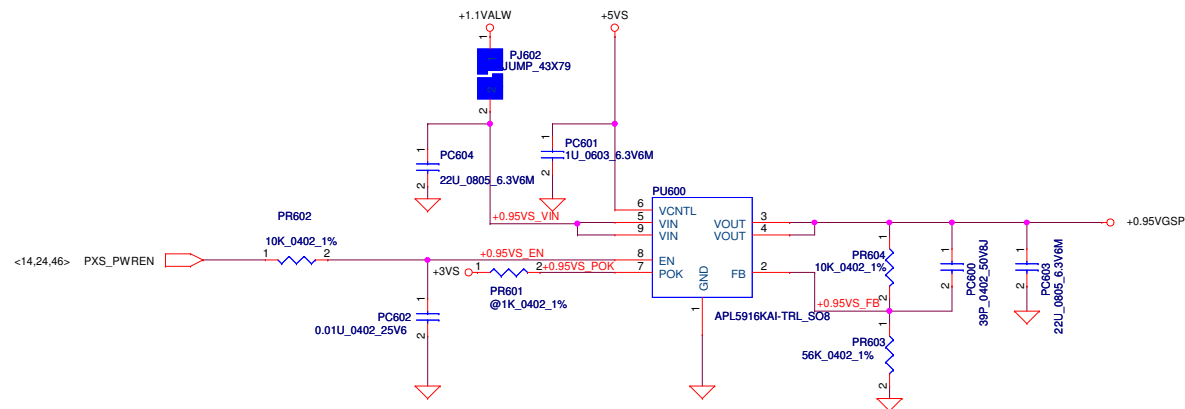


VGA controller (43.1),Driver (43.2) Support component (43.3)

EMI Part (47.1)



0.95V controller (35.11), Support component (35.12)

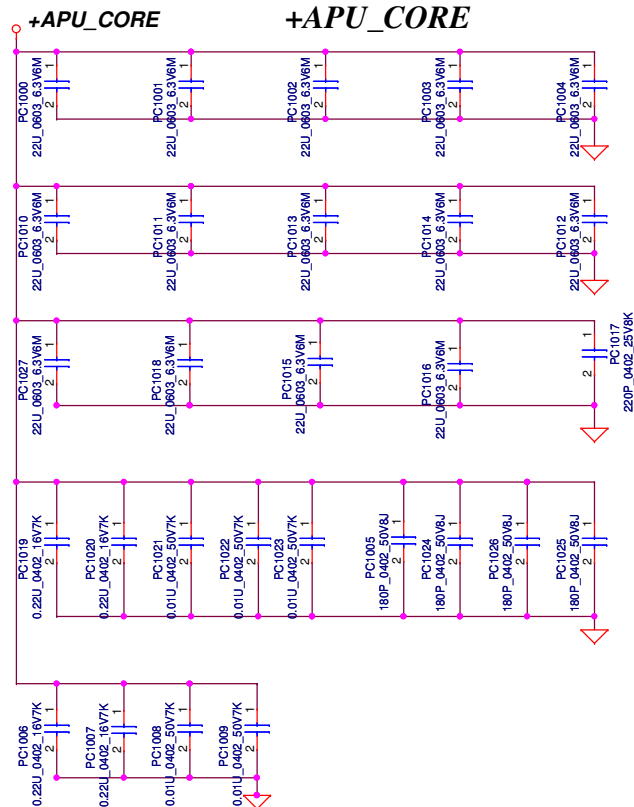


0.95v
 Peak Current 4A
 OCP current 16A
 FSW=800kHz

 H/S Rds(on) :22mohm ,
 L/S Rds(on) :11mohm ,

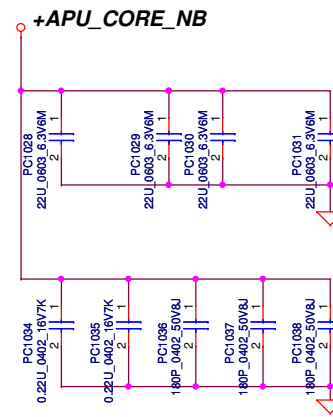
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/08/16				Deciphered Date			
2012/08/15				Title				+1.5VPCIE/0.935V			
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LA-9869P				Date				Wednesday, February 20, 2013			
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0.1											

CPU_Core output CAP (Including MLCC) 36.4



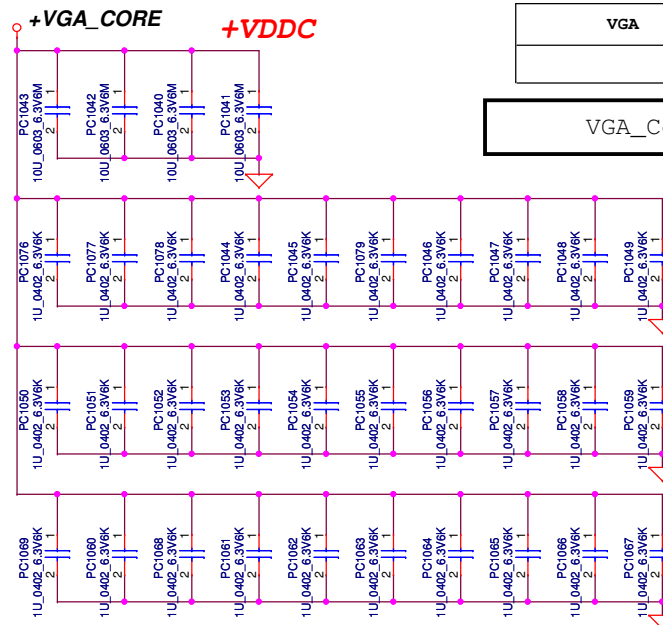
+APU_CORE_NB

GFX output CAP (Including MLCC) 36.5



Richland	330uF*9m	22uF	0.01u	0.22uF	180P
VDD	4	15	5	4	4
VDD_NB	1	4		2	3

+VGA_CORE



VGA	560u x1	10u x 4	1u x30

VGA_Core output CAP (Including MLCC) 43.9)

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/29	Deciphered Date	PROCESSOR DECOUPLING	
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Date: Wednesday, February 20, 2013			Sheet 48	Rev 0.1

Item	Reason for change	PG#	Modify List	Date	Phase
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Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)
1	EVT-2012/11/28	P39-PWR-BATTERY CONN / OTP	change PF2 vendor for cost down plane	PWR
2	EVT-2012/11/28	P41-PWR-+3VALW/5VALW	change PR337 235K to 210K & PR5357 156k to 174k	PWR
3	EVT-2012/11/28	P41-PWR-+3VALW/5VALW	Delate PC351 add PC353 150u D2 cap	PWR
4	EVT-2012/11/28	P43-PWR_+1.8VSGP/+1.1VALWP	change PC157 220u H=4.5mm to 330u D2 cap H=2mm	PWR
5	EVT-2012/11/28	P43-PWR_+1.8VSGP/+1.1VALWP	change PR158 16.2K to 17.4K	PWR
6	EVT-2012/11/28	P50-PWR-CPU_CORE	change the PC1101 560u to 330u	PWR

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Issued Date	2012/12/13	Deciphered Date	2013/12/13	Title	
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				Document Number VCUAA	
				Rev 0.2	
				Date: Wednesday, February 20, 2013	
				Sheet 49 of 50	

HW PIR (Product Improve Record)

VDKTE LA-9869P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2

GERBER-OUT DATE: 2012/12/25

Item	Page	Date	Request	Solution
1)	21	2012/12/04a	For CRT undershoot issue	Add R66 & R67 for CRT issue.
2)	14	2012/12/04a	For VGA_CORE display	unomunt CR103.
3)	22	2012/12/04a	For EMI request	Change L8/L9/L10/L11 part number for EMI request.
4)	34	2012/12/13a	For change EC PIN	Change 1.1VFWR_EN from pin 71 to pin 127 and USB_EN#0 from pin84 to pin 23.
5)	19	2012/12/14a	For LVDS translator	Delete all of RTD2132S components.
6)	31	2012/12/14a	For S&C port wake	Add CHG_PWR_GATE# on U15 pin 1 and connect to EC pin82.
7)	24	2012/12/17a	For leakage with PXS_PWREN	Change Power rail from +3VALW_FCH to +3VALW on R216 pin1
8)	07	2012/12/22a	For leakge	Delete R47, D18.
9)	24	2012/12/22a	For NV suggestion	Add R283 & Q30.
10)	34	2012/12/25a	For S&C port wake	Add RB25.

VDKTE LA-9869P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3

GERBER-OUT DATE: 2013/02/04

Item	Page	Date	Request	Solution
1)	24	2013/01/21a	For AMD suggestion	Update R288/R289 from 10K to 2.2K.
2)	22	2013/01/21a	For HDMIleakage issue	Change R571 to +3VS power rail.
3)	34	2013/01/21a	For Audio noise	Add EC_MUTE_INT (GPIO5D) and add RB38(0 ohm) and RB37 (4.7K PD)
4)	20	2013/01/21a	For layout routing	SWAP L56.
5)	20	2013/01/21a	For EMI request	Add R155/156.
6)	13	2013/01/28a	For Safety	Add GPU_DOWN# connect to EC.
7)	25	2013/01/29a	For EMI request	Add C508(10P)/R118(0 ohm) with FCH_SPI_CLK_R.
8)	33	2013/01/30a	For ESD request	Add D27~D30 on SPK.
9)	07	2013/01/30a	For ESD request	Add D31 on APU_PROCHOT#.
10)	20	2013/01/30a	For ESD request	Add D32 on Int mic clk/data and USB.
11)	34	2013/01/30a	For ESD request	Add DB2 on H_PROCHOT_EC.
12)	36	2013/01/31a	For move JTP	SWAP JTP
13)	24	2013/02/01a	For ESD request	Add 180p C505 on FCH_PWRGD.
14)	34	2013/02/01a	For ESD request	Add 180p CB17 on FCH_PWRGD.
15)	34	2013/02/04a	For PWR	Add GPIO pin 99 of EC for power.